

**Krishna V. Palem**  
*Rice University*  
*Kenneth and Audrey Kennedy Professor of Computing*  
*Department of Computer Science*

**I. RESEARCH INTERESTS**

*Adaptive architectures and computing, Algorithms, Compiler optimizations, Embedded systems, Low energy computing, Nanoelectronics.*

**II. EARNED DEGREES**

University of Texas, Austin, TX  
*Ph.D., August 1986*

University of Texas, Austin, TX  
*M.S. in Electrical and Computer Engineering (Biomedical Engineering), August 1981*

**III. EMPLOYMENT**

Aug 2007 – Present      **Rice University**  
*Kenneth and Audrey Kennedy Professor of Computing*  
*Department of Computer Science*  
*Professor, Electrical and Computer Engineering*  
*Director, VISEN Center,*  
*Director (designate) ISNE*

Feb 2000 – Present      **Georgia Institute of Technology**  
*Professor of Electrical & Computer Engineering*  
*Professor of Computer Science, College of Computing*  
*Senior Research Leader (funded),*  
*College of Engineering*  
*Director, Center for Research in*  
*Embedded Systems and Technology*

Dec 1999 – July 2003      **Procler Inc.**  
*Chief Technology Officer*

1994 – Dec 1999      **New York University**  
*Associate Professor, Courant Institute*  
*of Mathematical Sciences*

- 1986 – 1994                      **IBM T. J. Watson Research Center**  
*Research Staff Member*
- 1991 – 1994                      **IBM Santa Teresa Laboratory**  
*Advanced Technology Consultant*  
Advanced Development Technology Institute
- 1989 – 1993                      **New York University**  
*Visiting Member, Courant Institute*
- 1991 – 1994                      **Stanford University**  
*Visiting Scholar, Computer Science Department*

#### **IV. SELECTED RECOGNITION AND VISITING FELLOWSHIPS**

##### **Recognition and Fellowships**

1. *Moore Distinguished Faculty Fellow*, California Institute of Technology, 2006–07
2. Fellow of the ACM.
3. Fellow of the IEEE.
4. *Invited Professor*, Ecole Normale Supérieure, Paris, France, 2004 – 05.
5. *Outstanding Technology Nominee*, Analysts Choice Award in the field of Digital Processing, Proceler Inc, 2002.
6. *Schonbrunn Visiting Professor*, The Hebrew University, Jerusalem, Israel, 1999.
7. *Teaching Excellence*, The Hebrew University, Jerusalem, 1999.
8. *External Recognition Award*, IBM Research Division, 1994.

##### **Awards from Industry**

9. *Curricular Development Award*, Center for Research in Embedded Systems and Technology, Georgia Institute of Technology, Hewlett Packard Corporation, \$816,616. One of two awarded internationally (1999).
10. *Panasonic Research Award*, 1997– 98, \$100,000.
11. *Hewlett-Packard Research Award*, 1996–99, over \$900,000 cash, and \$400,000 equipment.

### **Student Supervision Awards**

1. Student S. Talla, *Janet Fabri Award for Outstanding Doctoral Thesis*, “Adaptive Explicitly Parallel Instruction Computing” May 2001, New York University.
2. Students A. Leung and S. Talla, *Harold Grad Prize*, April 1998 and *Dean’s Dissertation Fellowship*, September 1999, respectively, New York University.

### **V. GRANTS AND CONTRACTS**

\$2,800,000 for Institute for Sustainable NanoElectronics (ISNE), Singapore and its international network of excellence (current).

Total of over \$ 4,500,000 since 1999 from Federal agencies (of which about \$ 2,300,000 includes Co-PI’s A. Chatterjee, V. Mooney and S. Yalamanchili in different contracts)

### **VI. OTHER SCHOLARLY ACCOMPLISHMENTS**

1. Chaired the co-development of the Trimaran system ([www.trimaran.org](http://www.trimaran.org)) and led international dissemination. Trimaran has been used at over 40 universities in seven countries (1997-present).
2. Participated in the technology transfer of algorithms used in the ASTI module of the parallelizing front end in IBM’s C and Fortran compilers (1991–1994).

### **VII. RECENT PROFESSIONAL CONTRIBUTIONS**

#### **Conference/Editorial Activities**

1. Associate Editor, ACM Transactions on Embedded Computing Systems.
2. Editor, International Journal of Embedded Computing.
3. Guest co-editor (with Wen-mei Hwu) of the IEEE Transactions on Computers Special issue in memory of B. Ramakrishna (Bob) Rau.
4. Steering Committee member of CASES, 1999-present.
5. Program committee member, *CODES-ISSS 2005*.
6. Program committee member, *HPCA 2006*.

7. General Chair, *CASES 2001, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, Atlanta, GA. November 2001.
8. Chair, Scientific Advisory Board on *Use Inspired Research: Initiative in Embedded and Hybrid Systems*, Agency for Science, Technology and Research, Singapore, August 2001 - present.
9. Conference chair, *CASES 2000, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, San Jose, CA. November 2000.
10. Associate editor of *The IEEE Transactions on Parallel and Distributed Systems*, 1999 – 2003.
11. Founding Program co-chair, *CASES98, Workshop on Compiler and Architecture Support for Embedded Systems*, Washington, DC, October 1998.
12. Associate editor, *Constraints: An International Journal*, Kluwer, 1995–present.

### **Panelist Activity**

1. Agency for Science, Technology and Research, Singapore, 2001.  
*Chair, Emerging Directions in Embedded & Hybrid Systems*
2. NSF-DARPA Workshop Embedded Systems Panel, Washington, DC, 2000.  
*Chair, Future Directions in Hybrid and Embedded Systems*
3. National Science Foundation, Washington, DC, 1995.  
*Careers Panel*
4. National Science Foundation, Washington, DC, 1994.  
*Small Business Initiatives (SBIR) Panel*  
*Modeling Responsive Computing Systems: Compilation Issues*
5. National Science Foundation, Washington, DC, 1993  
*Young Investigator (NYI) Award Panel*

## **VIII. RECENT KEYNOTE AND INVITED PRESENTATIONS**

1. On “Probabilistic Low Energy Computing” at

- a. *Coolchips VII*, Sponsored by IEEE and ACM SIGARCH, Yokohama, Japan, Apr 2004.
  - b. *International Conference on High Performance Computing*, Sponsored by IEEE and ACM SIGARCH, Hyderabad, India, Dec 2003.
  - c. *Conference on Compilers, Architectures and Synthesis of Embedded Systems*, Sponsored by ACM SIGMICRO and IEEE, San Jose, CA, Oct 2003.
2. On “Adaptive EPIC Processors and Compilation Techniques,” *Application-Specific Multi-Processor SoC, Summer school sponsored by IEEE Circuits and Systems Society and EDAA*, July, 2001, Aix-les-Bains, France.
3. NSF-DARPA Workshop on “Compilers, Architectures and Synthesis of Embedded Systems,” Washington DC, October 2000.
4. “Trimaran: An Infrastructure for Research in Instruction Level Parallel Processing,” (with Ben Goldberg, Hansoo Kim and other Trimaran participants at
  - a. The 1998 Symposium on Parallel Architectures and Compiler Techniques (PACT), Paris, France, October 1998.
  - b. The 1998 ACM Symposium on Programming Language and Implementation (PLDI), Atlanta, GA, May 1999.
  - c. The School on Computational Aspects and Applications of Hybrid Systems, Grenoble, France, October 1998.
5. “Master Class in Reconfigurable Systems,” Adelaide, Australia, September 1998.

## **IX. GRADUATE STUDENT SUPERVISION**

### **INDIVIDUAL STUDENT GUIDANCE**

#### **Current Ph.D. Students**

1. Yogesh Chobe, Georgia Institute of Technology, School of Electrical & Computer Engineering, “Compiler Assisted Design Space Exploration and SoC Design”.
2. Romain Cledat, Georgia Institute of Technology, School of Electrical & Computer Engineering, “Geometry Aware Compiler Optimizations”.
3. Pinar Korkmaz, Georgia Institute of Technology, School of Electrical & Computer Engineering, “Program Optimizations for Management Power in the Memory Subsystem,” (joint with V. Mooney).
4. Lakshmi Chakrapani, Georgia Institute of Technology, College of Computing, “Probabilistic Architectures”.
5. Charles Hardnett, Georgia Institute of Technology, College of Computing, “Loop Transformations for Locality Enhancement”.

6. Allen Leung, New York University, “Compiler Optimizations and their Interactions with Garbage Collection with Applications to Java,” Ph.D, began advising: September 1995, Status: Defended thesis March 2001; Pending final submission of dissertation.

### **Graduated Ph.D. Students**

1. Rodric Rabbah, Georgia Institute of Technology, College of Computing, “Compiler Optimizations for Profile Based Management of the Memory Hierarchy,” Graduated: 2003, Employed: Massachusetts Institute of Technology, Cambridge, MA.
2. Jinwoo Kim, Georgia Institute of Technology, College of Computing, “Hardware Support of Compiler Optimizations for Smart Cache Management,” Graduated: 2003. Employed: City University of New York, New York, N.Y
3. Suren Talla, New York University, Courant Institute, “Adaptive EPIC Architectures and their Compilers,” Ph.D., Graduated May 2001. Employed: StarCore, Atlanta, GA.
4. Hansoo Kim, New York University, “Region Based Register Allocation,” Ph.D., graduated August 2000. Employed: Citibank, New York, NY.
5. S. Muthukrishnan, New York University, “Algorithms for String and Pattern Matching,” (joint with J. Spencer), Ph.D., Graduated: 1992, Employed: Rutgers University, New Brunswick, NJ.
6. P. Ouyang, New York University, “Compiling Regular Loops for Efficient Parallel Execution”, Ph.D., Graduated: 1990, Employed: Synopsis Corporation, San Jose, CA.
7. L. Ke, New York University, “Rewriting Systems,” Ph.D., Graduated: 1989, Employed: Fujitsu Corporation, San Jose, CA.

## **X. TEACHING**

### **Curriculum Development, Georgia Institute of Technology**

As part of the Center for Research in Embedded Systems and Technology, a three-course sequence has been developed on Modern Computer Architecture, Optimizing Compilers, and in Pervasive Computing. The first two of these courses, i.e., architectures and compilers were taught first at New York University and are now offered at the Georgia Institute of Technology. *Compiler Design: Optimizations for Modern Processors* was offered during the Fall 2000 semester and *High Performance Computer Architecture: The EPIC Approach* was offered during the Spring semester 2001. The third course entitled, *Designing Pervasive Computing Environments*, was offered during the Fall 2001 semester. The courses are evaluated, sponsored, and co-developed with the Hewlett Packard Corporation.

1. **Designing Pervasive Computing Environments**, (ECE8833A, also cross-listed as a graduate course in the College of Computing as CS8803.)
2. **High Performance Computer Architecture: The EPIC Approach:** (ECE 8833, also cross-listed as a graduate course in the College of Computing as CS 8803K EPIC Architectures.)
3. **Compiler Design: Optimizations for Modern Processor:** (ECE 8833A, also cross-listed as a graduate course in the College of Computing as CS 6241 Compiler Design).

### **Curriculum Development, New York University**

1. Introduced an advanced course, *Code Optimization in Modern Compilers*. This course was offered as G22.3033.01 *Optimizing Compilers* and G22.2131.001 *Advanced Topics In Compilers* and G22.3033.008 *Optimizing Compilers*. It is the basis for the Hewlett Packard Curriculum Development Award and is the foundation for the new course offered during the Fall 2000 semester at the Georgia Institute of Technology.
2. Developed a new Graduate Operating Systems course and 500 pages of lecture notes, jointly with Professor Malcolm Harrison.
3. Initially developed and offered as G22.3250.001 *Honors Operating Systems*, Fall 1996.

### **Short Courses**

1. Short course on “Code Optimization in Modern Compilers” offered at Tata Institute, Bombay, India, and with Vivek Sarkar, via the Western Institute of Computer Science, Stanford University, Palo Alto, 8/94, 8/95 and 8/96. This course was co-developed with V. Sarkar and served as the foundation for subsequent courses on optimizing compilers.

## **XI. SELECT CAMPUS CONTRIBUTIONS**

### **Georgia Institute of Technology Committee and Service Activities**

1. *Seminar Committee*, 2000 – 2001.
2. *Farmer Chair Search Committee*, 2000 - 2003.

3. *Motorola Chair Search Committee*, 2001 – 2002.
4. Director, *Center for Research in Embedded Systems and Technologies (CREST)*, 2000-present.

#### **New York University Committee and Service Activities**

1. *Graduate Student Fellowship Committee*, 1997 – 1998
2. *Faculty Appointments Committee (Tenure and Promotions Committee)*, 1997 – 1999

## **XII. PUBLICATIONS**

1. “Advocating Noise as an Agent for Ultra Low-Energy Computing: Probabilistic CMOS Devices and their Characteristics,” with P. Korkmaz, B. E. S. Akgul and L. N. Chakrapani, *to appear in Japanese Journal of Applied Physics, SSDM Special Issue Part 1*.
2. “A Review on Probabilistic CMOS (PCMO) Technology: From Device Characteristics to Ultra Low-Energy SoC Architectures,” with L. N. Chakrapani, B. E. S. Akgul and P. Korkmaz, *to appear in High Performance Embedded Computing Handbook: A Systems Perspective*.
3. “Ultra Efficient Embedded SoC Architectures based on Probabilistic CMOS (PCMO) Technology,” with L. N. Chakrapani, B. E. S. Akgul, S. Cheemalavagu, P. Korkmaz and B. Seshasayee, *to appear in The Proceedings of The 9th Design Automation and Test in Europe (DATE)*, March 2006.
4. “Ultra-low Energy Computing with Noise: Energy-Performance-Probability Trade-offs,” with P. Korkmaz and B. E. S. Akgul, *to appear in IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Karlsruhe, Germany*, March 2006.
5. “A Probabilistic CMOS Switch and its Realization by Exploiting Noise,” with S. Cheemalavagu, P. Korkmaz, B. E. S. Akgul and L. N. Chakrapani, *Proceedings of The IFIP-International Conference on Very Large Scale Integration, Perth, Australia*, October 2005.
6. “Data Trace Cache: An application specific cache architecture,” with S. Ramaswamy, J. Sreeram and S. Yalamanchili, *2005 Workshop (Memory performance: Dealing with Applications, systems and architecture), Saint Louis, Missouri*, September 2005.
7. “The Explicit Use of Probability in CMOS Designs and the ITRS Roadmap: From Ultra-low Energy Computing to a Probabilistic Era of Moore's Law for CMOS (invited),” with B. E. S. Akgul, *Cavin's Corner at Semiconductor Research Corporation (SRC)*, September 2005.

8. "Realizing Ultra-low Energy Application Specific SoC Architectures through Novel Probabilistic CMOS (PCMOS) Technology," with L. N. Chakrapani, B. E. S. Akgul and P. Korkmaz, *Proceedings of the 2005 International Conference on Solid State Devices and Materials (SSDM)*, Kobe, Japan, September 2005.
9. "Energy Aware Computing Through Probabilistic Switching: A Study of Limits," *IEEE Transactions on Computers Volume 54(9)*, pp. 1123-1137, September 2005.
10. "A Framework For Compiler Driven Design Space Exploration For Embedded System Customization (invited)," with L. N. Chakrapani and S. Yalamanchili, *Proceedings of the Ninth Asian Computing Science Conference, In Lecture Notes in Computer Science, Springer-Verlag, Volume 3321, Pages 395-406*, December 2004.
11. "Ultra Low-energy Computing via Probabilistic Algorithms and Devices: CMOS Device Primitives and the Energy-Probability Relationship," with S. Cheemalavagu, P. Korkmaz, *Proceedings of The 2004 International Conference on Solid State Devices and Materials (SSDM)*, Tokyo, Japan, September 2004.
12. "Adaptive Compiler Directed Prefetching for EPIC Processors," with J. Kim, R. Rabbah, W. Wong, *International Multiconference in Computer Science and Computer Engineering*, Las Vegas, NV, June 2004.
13. "Low Energy Computing: From Novel Semiconductor Devices to Applications, Models, and Moore's Law (invited)," *Coolchips VII*, Yokohama, Japan, Apr 2004.
14. "Trimaran: An Infrastructure for Research in Instruction-Level Parallelism," with L. N. Chakrapani, J. C. Gyllenhaal, W-M. W. Hwu, S. A. Mahlke and R. M. Rabbah, *Proceedings for the 17<sup>th</sup> International Workshop on Languages and Compilers for Parallel Computing*, 2004, *In Lecture Notes in Computer Science, Springer-Verlag, Volume 3602, Pages 32-41*, 2005.
15. "Data Remapping for Design Space Optimization of Embedded Memory Systems," with R. Rabbah. *ACM Transactions on Embedded Systems, Volume: 2 (2) pages 186 – 218*, May 2003.
16. "Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices," *International Conference on High Performance Computing*, Hyderabad, India, Dec 2003. Also appeared as: "Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices," *Proceedings of The Intl. conference on compilers, architecture and synthesis for embedded systems (CASES)*, 2003.
17. "Energy minimization of a pipelined processor using a low voltage pipelined cache," with Park, J.C.; Mooney, V.J., III, K.; Kyu-won Choi. *Thirty-Sixth Asilomar Conference on Signals, Systems and Computers*, Nov 2002.
18. "Software Bubbles: Using Predication to Compensate for Aliasing in Software Pipelines," with B. Goldberg, E. Crutcher, C. Huneycutt, *International*

- Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2002.
19. "Proof as Experiment: Algorithms from a Thermodynamic Perspective", *Proceedings of The Intl. Symposium on Verification (Theory and Practice)*, Taormina, Sicily, Italy, July 2003.
  20. "Design Space Optimization of Embedded Memory Systems via Data Remapping," with Rodric M. Rabbah, Vincent Mooney III, Pinar Korkmaz and Kiran Puttaswamy. *In Proceedings of the Languages, Compilers, and Tools for Embedded Systems and Software and Compilers for Embedded Systems (LCTES-SCOPES)*, June 2002.
  21. "A Framework for Data Prefetching Using Off-Line Training of Markovian Predictors," with J. Kim, W. Wong. *20th International Conference on Computer Design*, Germany, 2002.
  22. Power-Performance Trade-Offs in second level memory used by an ARM-Like RISC Architecture," with K. Puttaswamy, L. N. Chakrapani, K. W. Choi, Y. S. Dhillon, U. Diril, P. Korkmaz, K. K. Lee, J. C. Park, A. Chatterjee, P. Ellervee, V. Mooney and W. F. Wong in the book *Power Aware Computing*, edited by Rami Melhem, University of Pittsburgh, PA, USA and Robert Graybill, DARPA/ITO, Arlington, VA, USA, published by Kluwer Academic/Plenum Publishers, pp. 211-224, May 2002
  23. The Emerging Power Crisis in Embedded Processors: What Can A Poor Compiler Do?," with L.N. Chakrapani, P. Korkmaz, V.J. Mooney III, and W.F. Wong, *Proc. of International Conference on Compilers, Architectures, and Synthesis of Embedded Systems*, Nov 2001.
  24. "Compiler Optimizations for Adaptive EPIC Processors," with S. Talla, W. Wong. *First International Workshop on Embedded Software (EMSOFT)*, Tahoe City, CA, 2001.
  25. "Connectivity Properties in Random Regular Graphs with Edge Faults", with S. Nikolettseas, P. Spirakis and M. Yung, *Special Issue on Randomized Computing of the International Journal of Foundations of Computer Science (IJFCS)*, 2000.
  26. "Instruction Scheduling with Timing Constraints on Single RISC Processor with 0/1 Latencies," with H. Wu, J. Jaffar and R. Yap. *Sixth International Conference on Principles and Practice of Constraint Programming*, Singapore, 2000.
  27. "Emerging Application Domains and the Computing Fabric (invited)," *Advances in Computing Science - ASIAN'99: 5th Asian Computing Science Conference, Phuket, Thailand*, December 1999.
  28. "Adaptive Explicitly Parallel Instruction Computing," with S. Talla, P. Devaney, et.al., *Fourth Australasian Computer Architecture Conference*, Auckland, New Zealand, January 1999.
  29. "Scheduling Time-Constrained Instructions in Pipelined Processors," with A. Leung and A. Pnueli. *ACM Transactions on Programming Languages and Systems*, October 2000. Also appeared as: "A Fast Algorithm for Scheduling Time-constrained Instructions in RISC Machines," *Proc. 1998 Symposium on Parallel Architectures and Compiler Techniques*, Paris, France, October 1998.

30. "TimeC: A Time Constraints Language for ILP Processor Compilation," with A. Leung and A. Pnueli, *Constraints*, August 2000. Also appeared as: "TimeC: A Notation for Expressing Time-constraints in Programs," *Proc. The Fifth Annual Australasian Conference on Parallel and Real-time Systems*, Adelaide, Australia, September 1998.
31. "Efficient Dictionary Matching in Parallel," with S. Muthukrishnan, *SIAM J. Computing*, letter of acceptance subject to revision received in 1998.
32. "Seeking Solutions in Configurable Computing," with W. H. Mangione-Smith, B. Hutchings, D. L. Andrews, A. DeHon, C. Ebeling, R. W. Hartenstein, O. Mencer, J. Morris, V. K. Prasanna, and H. Spaanenburg, *IEEE Computer*, 30(12), pp. 38-43, December 1997.
33. "Run-time versus Compile-time Instruction Scheduling in Superscalar (RISC) Processors: Performance and Trade-off," with Allen Leung and Cristian Ungureanu, *Journal of Parallel and Distributed Computing*, 45(1), pp. 13-28, 1997.
34. "End-to-End Solutions for Reconfigurable Systems: The Programming Gap and Challenges," *Proceedings of the Hawaii International Conference on Systems and Sciences*, January 1997.
35. "Very Efficient Cyclic Shifts on Hypercubes," with P. Ouyang, *Journal of Parallel and Distributed Computing*, 39(1), pp. 79-86, 1996. Also appeared as: "Very Efficient Cyclic Shifts on Hypercubes," *Proc. 3rd IEEE Symposium on Parallel and Distributed Processing*, Dallas, TX, December 1991.
36. "Optimal Parallel Suffix-prefix Matching Algorithm and Applications," with Z. Kedem and G. Landau, *SIAM J. Computing*, 25(5), pp. 998-1023, 1996. Also appeared as: "Optimal Parallel Suffix-prefix Matching Algorithm and Applications," *Proc. 1st Annual ACM Symposium on Parallel Algorithms and Architecture*, Santa Fe, NM, pp. 388-398, July 1989.
37. "Tail Bounds for Occupancy and the Satisfiability Threshold Conjecture," with A. Kamath, R. Motwani, P. Spirakis. *Random Structures and Algorithms*, Vol. 7, pp. 59-80, 1995. Also appeared as: "Allocation Bounds and Thresholds for (Un)Satisfiability," *Proc. 35<sup>th</sup> Annual IEEE Symposium on FOCS*, Santa Fe, NM, November 1994.
38. "Faulty Random Graphs," with P. Spirakis, M. Yung and P. Zaroliagis, *International Conference on Automata Languages and Programming*, Jerusalem, Israel, July 1994.
39. "Non-standard Stringology: Algorithms and Complexity," with S. Muthukrishnan, *26th Annual ACM Symposium on the Theory of Computing*, Montreal, Canada, pp. 770-779, May 1994.
40. "Highly Efficient Asynchronous Execution of Large-Grained Parallel Programs," with Y. Aumann, Z. Kedem and M. Rabin, *34th IEEE Conf. on Foundations of Computer Science*, Palo Alto, CA, pp. 271-280, November 1993.
41. "Efficient Dictionary Matching in Parallel," with S. Muthukrishnan, *Proc. 5th Annual ACM Symposium on Parallel Algorithms and Architecture*, Saarbrücken, Germany, pp. 69-78, June 1993.

42. "An Efficient Parallel Algorithm for Anti-unification," with G. Kuper, K. McCaloon and K. Perry, *Journal of Automated Reasoning*, 9(3), pp. 381-389, 1993. Also appeared as: "Efficient Parallel Algorithms for Anti-Unifications and Relative Complement," in *Proc. Third IEEE Symposium on Logic in Computer Science*, Edinburgh, Scotland, pp. 112-120, July 1988.
43. "Scheduling Time-Critical Instructions on RISC Machines," with B. Simons, *ACM Transactions on Programming Languages and Systems*, vol. 15, pp. 632-658, 1993. Also appeared as: "Scheduling Time-Critical Instructions on RISC Machines," *Proc. ACM Symposium on Principles of Programming Languages*, San Francisco, CA, pp. 270-280, January 1990.
44. "Optimal Parallel Algorithms for Forest and Term Matching," with Z. Kedem, *Theoretical Computer Science*, vol. 93, pp. 245-264, 1992.
45. "Resilient Parallel Computation," with Z. Kedem, *Proc. 2nd IEEE Workshop on Fault-tolerant Parallel and Distributed Systems*, Amherst, MA, July 1992.; Also appeared as: "Resilient Parallel Computing," in *Trends in Parallel Computation: vol. II*, P. Gibbons and P. Spirakis (eds), Cambridge, MA 1992; Also appeared as: "Efficient Program Transformations for Resilient Parallel Computation via Randomization," *Proc. 24th ACM Symposium on Theory of Computing*, pp. 306-317, May 1992.
46. "Instruction Scheduling," with B. Simons (invited), in *Optimizing Compilers*, F. Allen, B. Rosen and K. Zadeck (eds), Addison-Wesley; chapter revised and submitted to editors in 1992 and documented as an IBM Technical Report.
47. "Fast Parallel Algorithms for Coloring Random Graphs," with Z. Kedem, G. Panziou, P. Spirakis and K. Zaroliagis, *Proc. 17th International Workshop on Graph Theoretic Concepts in Computer Science*, Austria, pp. 135-147, June 1991.
48. "Combining Tentative and Definite Executions for Very Fast Dependable Parallel Computing," with Z. Kedem, A. Raghunathan and P. Spirakis, *Proc. 23rd ACM Symposium on Theory of Computing*, New Orleans, LA, pp. 381-390, May 1991.
49. "Efficient Robust Parallel Computation," with Z. Kedem and P. Spirakis, *Proc. 22nd ACM Symposium on Theory of Computing*, Baltimore, MD, pp. 138-148, May 1990.
50. "On the Complexity of Precedence Constrained Scheduling," *TR-86-11*, Department of Computer Sciences, The University of Texas, Austin, TX, 1986.
51. "Image Processing Architectures: A Taxonomy and Survey," with S. Yalamanchili et al., in *Progress in Pattern Recognition, vol. II*, L. Kanal and A. Rosenfeld (eds.), North-Holland, Amsterdam, pp. 1-38, 1985.
52. "The Complexity of Scheduling Systems of Non-identical Processors," with D. S. Fussell, in *Proc. of the 15th Southeastern Conference on Combinatorics, Graph Theory and Computing*, Baton Rouge, LA, March 1984.
53. "Multichannel Real-Time Analysis of the Clinical EEG on a Dual Microprocessor System," with R. E. Barr, J. Bashyam, D. Messenger and P. Norwood, in *J. Clinical Engineering*, vol. 9, 1984.

54. "A Period-peak Algorithm for EEG Analysis," with R. E. Barr, in *Computer Programs in Biomedicine*, vol. 14, 1982.
55. "Analysis of Background EEG Activity on a 16-bit Microcomputer," with R. E. Barr, D. Messenger and P. Norwood, in *Proc. of the 3rd Annual Conference of the IEEE EMBS*, Houston, TX, pp. 290-293, September 1981.
56. "A Period-peak Algorithm for EEG Analysis" with R. E. Barr, in *Proc. of the 34<sup>th</sup> Alliance for Engineering in Medicine and Biology*, Houston, TX, pp.207, September 1981.