Characterizing the Behavior of a Probabilistic CMOS Switch Through Analytical Models and Its Verification Through Simulations

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1. ABSTRACT

Noise immunity and low-energy computing have become limiting factors in semiconductor roadmap as feature sizes shrink. By viewing noise as a resource rather than as an impediment, we present a new approach to low-energy computing. The subject of our study is the probabilistic CMOS *(*PCMOS*) inverter, whose behavior is rendered probabilistic by noise. Summarized through the concept of an energy-probability relationship for* CMOS *inverters based on* AMI $0.5\mu m$ *and* TSMC $0.25\mu m$ *processes, we quantitatively show that significant energy savings are possible when a probabilistic inverter is switched with probability* $1/2 < p < 1$*, and that these savings increase exponentially as* p *is lowered. We also quantitatively show that increasing the noise* RMS *has the effect of increasing energy per switching step quadratically. Furthermore, we demonstrate the effects of the noise bandwidth and the output sampling frequency on the probabilistic behaviour of* CMOS *inverters.*

2. INTRODUCTION

As CMOS devices scaling approach the nano-meter region, the impact of deep submicron noise has become an important challenge, especially due to noise being seen as an obstacle to reliable computation. Another significant challenge to CMOS design is achieving low energy consumption for CMOS circuits, which has traditionally been addressed by voltage scaling. However, the utility of voltage scaling is decreasing, because lowering the voltage levels, therefore bringing the signal level closer to the noise level reduces noise immunity, and leads to unreliable computing. In [3] and [4], as a paradigm shift from previous approaches to overcome these dual challenges to CMOS design, noise is viewed as a resource (rather than an impediment) for achieving low energy computing. In the heart of this new approach is a probabilistic switch or inverter, whose output is guaranteed to be correct only with a probability p, $0.5 < p < 1$. It was shown in [19] that by using the probabilistic inverter as a building block, the $energy \times performance$ metric at the application level can be improved upto a factor of 1900, for a probabilistic string classification application. In this context, it is crucial to understand the device level behavior of these probabilistic devices which serve as the key building blocks for probabilistic system-on-a-chip (SoC) implementations. Therefore, in this work, we provide a comprehensive characterization of a probabilistic CMOS (PCMOS) switch (inverter). Our study is centered on conventional inverters coupled with noise to induce the probabilistic behavior. We consider the thermal noise and power supply noise as the sources of randomness. Specifically, we characterize the probability of correctness (p) and the energy consumed per switching (E) of such an inverter, which we refer to as the E-p relationship.

Furthermore, we characterize the probabilistic behavior for two scenarios of thermal noise source, wherein the thermal noise is coupled to the input or the output of the inverter. In addition, we establish the impact of the equivalent bandwidth of the noise (see Section 8 for details) on the probabilistic behavior of the CMOS

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inverter. We also characterize the impact of the output sampling frequency on the probabilistic behavior of the CMOS inverter.

In Section 3, we provide a summary of the background for our work. Following this, we define the probabilistic switch in Section 4, wherein we also provide a CMOS implementation of the probabilistic switch (inverter). In Section 5, we present analytical models characterizing the E-p relationship of the probabilistic inverter, where we study both the thermal and power-supply noise sources plus the two different couplings of thermal noise. In Section 6, we validate our analytical models through comparisons of analytical results with the results of circuit simulations in HSpice. In Section 7, we provide an improved analytical model characterizing the E-p relationship, wherein we include the short-circuit energy consumption of the inverter in calculating the energy consumed by the inverter. In addition, we validate the improved analytical model via comparisons of the model results with the HSpice simulation results. In Section 8, we depict the impact of the equivalent bandwidth of the noise, and the output sampling frequency on the probabilistic behavior of the CMOS inverter. In Section 9, we show the effect of the spurious switchings resulting due to the input-coupled noise on the energy consumption of a CMOS inverter. We conclude the paper in Section 10.

3. BACKGROUND

Energy efficiency has become an important design criterion for CMOS circuits, especially due to the increasing ubiquity of mobile and portable applications. One common technique for reducing energy is reducing the supply voltage. For example, in [28], the effect of voltage supply and threshold voltage scaling on the energy and performance of a ring oscillator is studied. Similarly, Kuroda et al. [12] describe a variable supply voltage scheme, wherein the supply voltage is changed adaptively depending on the required frequency of operation. However, there are two drawbacks of reducing the supply voltage. One drawback is the increase in the delay of gates. To overcome this problem, the threshold voltage is also scaled (see [6, 28]). The other drawback of reducing the supply voltage is the degradation of noise immunity of the circuits [6]. In 2003 ITRS roadmap [9], for example, it is stated that increasing noise sensitivity has become an important issue in the design of devices, circuits and systems due to the reduction in operating voltage by 20% per technology node.

The reduction of the feature sizes leads to a decrease in the number of dopants and channel electrons in the active regions of the device [23]. There are random fluctuations in the physical quantities of the devices such as the channel current resulting from the dopants and channel electrons. From the central limit theorem [21], the magnitude of the random variations is inversely proportional to the number of random variables. Thus, as the devices shrink, the random variations become more prominent. Sano [23] has investigated the intrinsic current fluctuations in very small Si-MOSFETs using Monte Carlo device simulations and has found that the normalized standard deviation of the drain current increases as the device width is reduced to the deep submicron regime.

Starting from the early work of Stein [25], the limitations that noise is imposing on the scaling of supply voltage and switching energy consumption of the circuits have been studied. For example, Natori and Sano [15] have derived a minimum energy consumption-reliability relationship for practical electronic circuits and investigated the scaling limits imposed by thermal noise on digital MOS circuits. Similarly, Kish [10] has studied the potential difficulties of scaling with high density integration due to thermal noise and Hegde and Shanbhag [8] have derived information-theoretic lowerbounds on energy consumption of noisy digital gates.

Differing from the above approaches, that is, rather than treating noise as an impediment to overcome, but viewing it as a resource of randomness, Palem [17, 18] outlined a framework for probabilistic switches and computational models based on these switches. These probabilistic computational models were used to derive low-energy computational platforms for probabilistic algorithms [14]. Palem's work has shown that well-characterized noise is of significant value in realizing low-energy computing platforms for probabilistic applications.

In order to extend Palem's work to the CMOS domain, the relationships between the probability of a switching step being correct, p, and the operating voltage, as well as the amount of noise in the system, were studied by Cheemavalagu, Korkmaz and Palem [3]. In the center of this work is a CMOS inverter, whose probabilistic behavior is characterized as a function of the energy it consumes per switching. Subsequently, this work was extended in [4], wherein an extensive characterization of the relationships between the noise, operating voltage, the associated probabilistic behavior, and the energy consumed per switching step is presented. In this paper, we further extend these characterizations by considering different types of noise couplings. Our model has been improved to characterize the probabilistic behavior induced due to power supply noise (in addition to thermal noise). We also study the effect of the equivalent bandwidth of the noise, as well as the output sampling frequency on the probabilistic behavior.

4. DEFINITIONS AND CONCEPT

In this section, we first define the concepts of probabilistic switch and probabilistic switching. Then we introduce a CMOS inverter realization of the probabilistic switch.

4.1 Probabilistic Switch

We define a *switch* as a digital device with one input and one output. Our choice of the single input, single output device is due to the simplicity of the analysis. The output of the switch is a function, f, of the input of the switch. The *switching* is defined as the invocation of the function f, which also corresponds to the event when the output is computed. The switching takes finite amount of time T_s. The switch and its associated switching can be either deterministic or probabilistic. If we denote the output of the switch by $Y(t)$ and the input of the switch by $X(t)$, where t denotes time, then for a deterministic switch, $Y(t_2) = f(X(t_1))$, where f:{0,1}→{0,1} is a function of a single bit, t_2 is the point in time when the switching ends, and t_1 denotes the point in time when the switching starts. On the other hand, for a probabilistic switch,

$$Y(t_2) = \begin{cases} f(X(t_1)) & \text{with probability } p \ (1/2 < p < 1) \\ \overline{f(X(t_1))} & \text{with probability } 1-p \end{cases} \tag{1}$$

In Figure 1, we show a probabilistic switch and a mathematical equivalent of this probabilistic switch; for simplicity, the binary input is denoted by X and the binary output is denoted by Y (t is omitted). In the equivalent structure (shown on the righthand side of the figure), every switching is associated with a coin toss, and the outcome of the coin toss is denoted by j. The deterministic switch of the equivalent structure computes a function g with inputs X and j, and the output Y of this switch is

$$Y(t_2) = g(X, j, t_2) = \begin{cases} f(X(t_1)) & \text{if } j = T \\ \overline{f(X(t_1))} & \text{if } j = F \end{cases} \tag{2}$$

Since probability p is a real number between 1/2 and 1, the coin toss should be biased so that it can lead to values of p other than 1/2.

We will introduce the probabilistic CMOS inverter in the next section where a conventional CMOS inverter is coupled with external noise to produce a probabilistic CMOS inverter. The external noise coupled to the CMOS inverter can be associated with the input j that is shown in Figure 1. However, when we describe the energy consumption associated with the probabilistic inverter (in Section 5), we do not consider any additional energy cost due to the generation of j, that is the generation of the external noise in the context of the probabilistic CMOS inverter. We note that, in the current report, the external noise coupled to the CMOS inverter is a Gaussian random process.

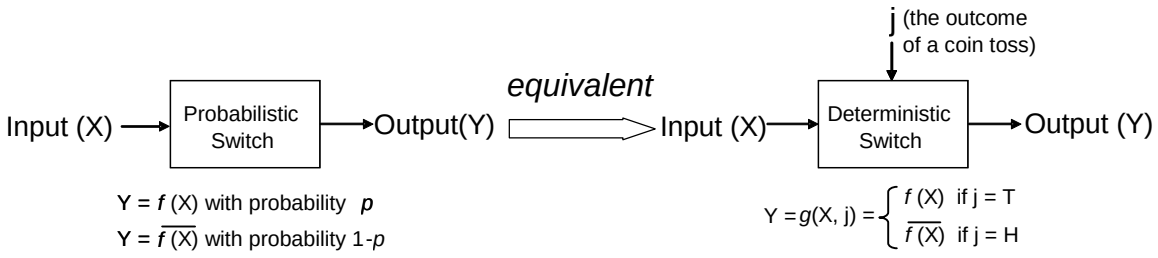

Figure 1. Definition of a probabilistic switch

4.2 CMOS Inverter Realization of a Probabilistic Switch

A CMOS inverter is a digital gate that executes the *inversion* function with one input and one output. The switching in this case is the invocation of the inversion function, which, in the context of the CMOS inverter, corresponds to the flow of the switching current through the output capacitance of the inverter. In the context of the switch described in Section 4.1, for a deterministic inverter, $Y(t_2) = \overline{X(t_1)}$ where Y and X denote the binary values of the output and the input of the inverter, respectively, t_2 denotes the point in time when the switching ends, and t_1 denotes the point in time when the switching starts. In addition, the switching time $T_s = (t_2 - t_1)$ is equivalent to the propagation delay of the inverter. For a probabilistic inverter, on the other hand,

$$Y(t_2) = \begin{cases} \overline{X(t_1)} & \text{with probability } p \ (1/2 < p < 1) \\ X(t_1) & \text{with probability } 1\text{-}p \end{cases} \tag{3}$$

In this paper, the probability p results from the noise coupled to the CMOS inverter. For example, Figure 2(c) shows the output waveform of a CMOS inverter which is coupled with thermal noise at its input and has a probability parameter $p = 0.89$. Because of the noise, the output voltage of the inverter undergoes transitions to binary 0, while it should be at binary 1, and vice versa. Figures 2(a) and (b) show the input and output waveforms of a deterministic CMOS inverter, respectively.

Noise in digital CMOS ICs can be modeled as coming from the evaluation nodes (input/output), power lines, or ground lines [24]. In Section 5.1, we characterize the probabilistic behavior of a CMOS inverter, wherein we consider the thermal noise coupled to the input or the output of the inverter as shown in Figure 3. In Section 5.2, we depict the impact of power supply noise on the probabilistic behavior of the CMOS inverter. The thermal and power supply noise sources are random processes that are characterized by a Gaussian distribution.

We note that, in Figure 2, the input and output of the CMOS inverter, denoted by V_{in} and V_{out}, respectively, are continuous signals. However, the mathematical definition of the probabilistic inverter, which is provided in (3), is based on binary input and output signals. Hence, it is necessary to define the binary equivalents of the continuous input and output signals. For the sake of simplicity, we assume that the transfer characteristics of the CMOS inverter is idealized as shown in Figure 4(a) as opposed to the realistic transfer characteristics, which is shown in Figure 4(b). Using this idealized transfer characteristics, the binary input and output values X and Y associated with the continuous input and output signals (V_{in} and V_{out}) of the CMOS inverter are defined as follows:

$$Y(t) = \begin{cases} 1 & \text{if } V_{out}(t) \geq V_m \\ 0 & otherwise \end{cases} \tag{4}$$

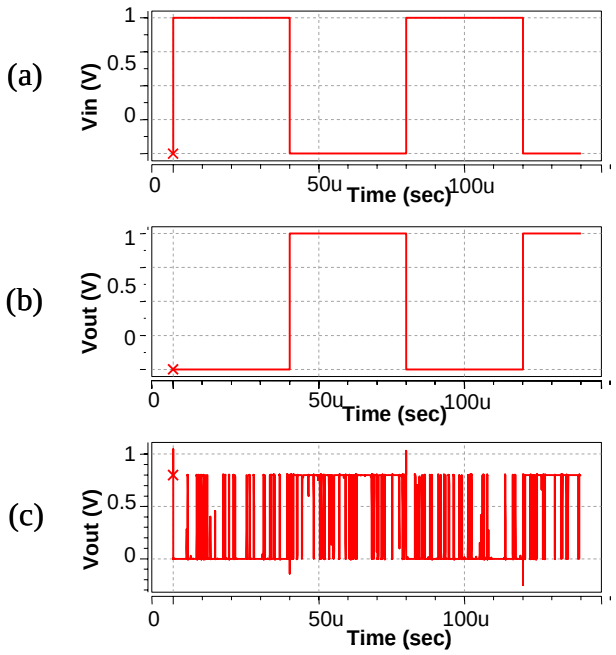

Figure 2. (a) Input voltage of a deterministic CMOS inverter (b) Output voltage of as deterministic CMOS inverter (c) Output voltage of a probabilistic CMOS inverter with probability parameter $p = 0.89$ for the same input

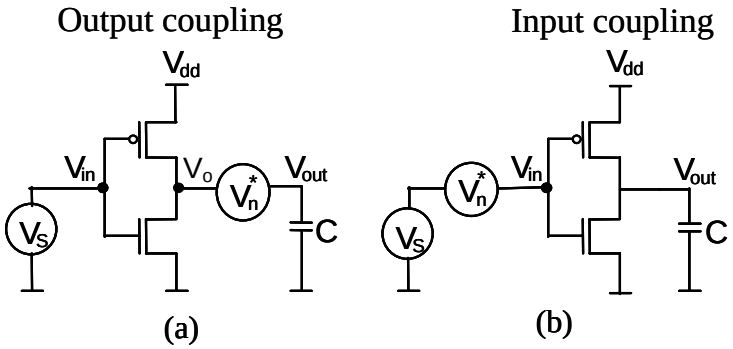

Figure 3. The two ways in which thermal noise is coupled to a deterministic inverter yielding its probabilistic variant

$$X(t) = \begin{cases} 1 & \text{if } V_{in}(t) \geq V_m \\ 0 & otherwise \end{cases} \tag{5}$$

In equations (4) and (5) V_m denotes the midpoint voltage of the CMOS inverter, which is defined as the point where the output voltage of the inverter becomes the same as the input voltage of the inverter during switching (see Figure 4(b)).

We idealize the transfer characteristics of the CMOS inverter as shown in Figure 4(a), because the use of this

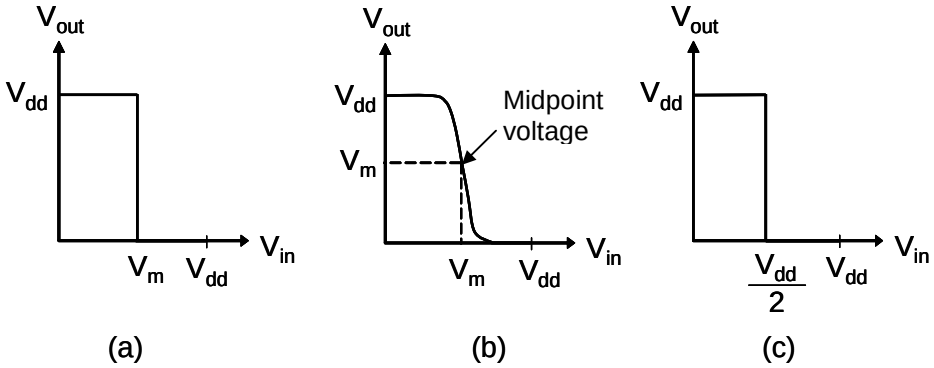

Figure 4. (a) Our idealization to the transfer characteristics of a CMOS inverter (b) Realistic transfer characteristics of a CMOS inverter (c) Traditional ideal transfer characteristics of a CMOS inverter when $V_m = \frac{V_{dd}}{2}$

idealization in deriving the probabilistic behavior has provided reasonable accuracy when analytical results are compared against the simulation results wherein accuracy is defined as the degree of the closeness of the analytical results to the simulation results. We note that, this idealization has resulted in slightly better accuracy than the traditional idealization of the transfer characteristics of the CMOS inverter (see Figure 4(c)).

5. CHARACTERIZATION OF THE PROBABILISTIC BEHAVIOR OF A CMOS INVERTER

As stated in Section 4.2, the probabilistic behavior of a CMOS inverter is induced by the noise coupled to it. In the current paper, we consider the thermal noise sources coupled to the input or the output of the inverter (see Figure 3) and the power supply noise on the power supply (V_{dd}) line. In Section 5.1 below, we present the analytical model characterizing the probability parameter p of a CMOS inverter when thermal noise is coupled to its input or output. In Section 5.2, we model the impact of power supply noise on the probabilistic behavior of the CMOS inverter. In Section 5.3, we establish the E-p relationship of a probabilistic inverter, which characterizes the energy consumed by a PCMOS inverter per switching step as a function of its probability parameter p.

5.1 Analytical Modeling of the Probability Parameter (p) of a PCMOS Inverter with Input- or Output-coupled Thermal Noise

In the cases that the noise is coupled to the input or the output of the inverter (see Figure 3), we use the approximations shown in Figure 5, wherein the inverter is approximated as an ideal switch in series with a resistor and a capacitor to simplify the analysis. Similar approximations of an inverter were used in [25, 15, 10]. In this approximation, the resistor R is the effective on-resistance of each transistor [15] and the capacitor C corresponds to the output capacitance of the inverter. We assume that the ideal switch switches at V_m which corresponds to the midpoint voltage of the CMOS inverter as explained before in Section 4.2.

In the case that thermal noise is coupled to the output of the CMOS inverter, referring to Figure 5(a), the input voltage (V_{in}) controls the position of the ideal switch. However, in the case that thermal noise is coupled to the input of the inverter, the position of the ideal switch is controlled by $V_s + {V_n}^*$ wherein V_s denotes the noise-free part of the input voltage and ${V_n}^*$ denotes the noise voltage. In the sequel, we will derive an analytical expression modeling the probability parameter of a CMOS inverter using the approximations shown in Figure 5.

Referring to the mathematical definition of the probabilistic inverter provided in Section 4, the switching time T_s corresponds to the RC delay of the approximated circuit. In this section we do not consider the (low-

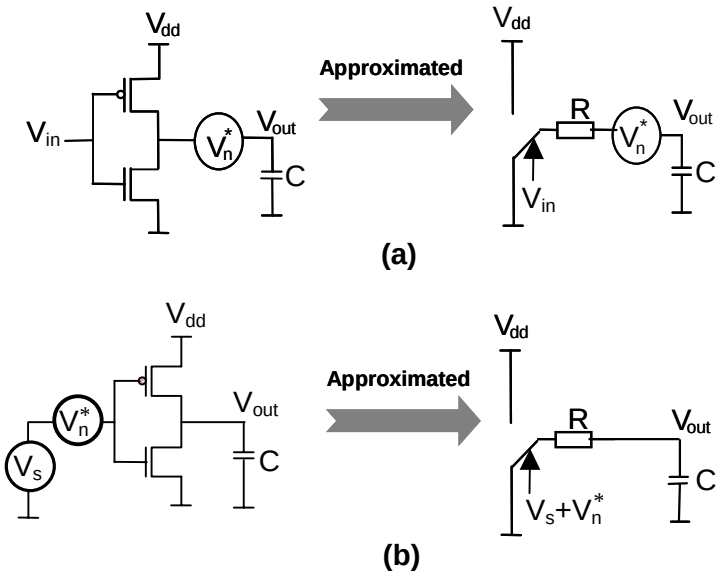

Figure 5. The approximations to a CMOS inverter (a) when thermal noise is coupled to inverter's output (b) when thermal noise is coupled to inverter's input

pass) filtering impact of the RC network on the noise. We assume that the noise is sampled at the beginning of the switching and held at the sampled value during switching; and the sampling period of the noise is larger than T_s. Hence, in the case of input-coupled noise, an error that occurs at the input of the inverter propagates to the output of the inverter. In addition, we assume that V_{out} is sampled at the same period as the noise is sampled. We refer to the sampling period of the noise as t_{sn}, and the sampling period of V_{out} as t_{so}. These assumptions on t_{sn} and t_{so} are valid throughout the current section. Later, in Section 8, we will revisit this topic, and study the filtering impact of the RC network as well as the impact of varying t_{sn} and t_{so} on the probabilistic behavior of the inverter.

In this paper, to model the thermal noise and power supply noise, respectively, by following the approach of [25] and [20], we assume that our noise sources are random processes that are characterized by Gaussian distribution with standard deviation σ. We refer to σ as the root mean square (RMS) value of the noise.

The noisy output (input) voltage V_{out} (V_{in}) is represented as two Gaussian curves each of which has a standard deviation of σ as shown Figure 6. More specifically, when the binary value of the output (input) is 1 (corresponding to the curve on the right), the mean value of the output (input) voltage is V_{dd} Volts, whereas when the binary value of the output (input) is 0, corresponding to the curve on the left, the mean value of the output (input) voltage is 0 Volt. The probability of the output (input) digital value 0 being treated as 1 is represented by the shaded area under the two Gaussian curves. Similarly, the probability of the output (input) digital value 1 being treated as 0 is represented by the unshaded area under the two Gaussian curves. In the case of output-coupled noise, the probability of 1 being treated as 0 (e_{10}) and probability of 0 being treated as 1 (e_{01}) are described by

$$e_{10} = \int_{-\infty}^{V_m} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(x - V_{dd})^2}{2\sigma^2}\right) dx \tag{6}$$

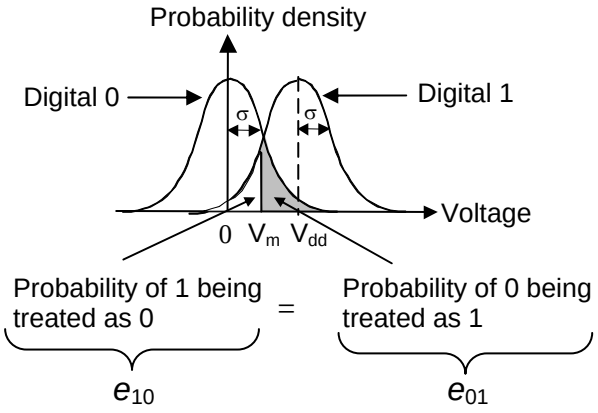

Figure 6. The digital values 0 and 1 represented by the two Gaussian curves

$$e_{01} = \int_{V_m}^{\infty} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{x^2}{2\sigma^2}\right) dx \tag{7}$$

On the other hand, when the thermal noise is input-coupled, e_{10} is represented by (7) and e_{01} is represented by (6) since the errors e_{10} and e_{01} are associated with the output voltage, which is identical to the "inverse" of the input voltage.

The probability of being correct (p) is equal to the average value of probability of being correct for the switchings from 1 to 0 and 0 to 1 and described by

$$p = 1 - \frac{e_{01} + e_{10}}{2} \tag{8}$$

Replacing the integrations of (6) and (7) into (8) yields the following relationship between p and V_{dd}, wherein p is the probability of being correct for a CMOS inverter that is either input- or output-coupled with thermal noise with an RMS value of σ.

$$p = \frac{1}{2} + \frac{1}{4} erf\left(\frac{V_m}{\sqrt{2}\sigma}\right) + \frac{1}{4} erf\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma}\right) \tag{9}$$

In (9) erf is the error function defined as $erf(x) = 2/\sqrt{\pi} \int_0^x e^{-u^2} du$ for a real number x. V_m, as stated before, is the midpoint voltage of the inverter, and expressed as follows:

$$V_m = \frac{V_{dd} - |V_{Tp}| + \sqrt{\frac{\mu_n}{\mu_p} \cdot \frac{(W/L)_n}{(W/L)_p}} \cdot V_{Tn}}{1 + \sqrt{\frac{\mu_n}{\mu_p} \cdot \frac{(W/L)_n}{(W/L)_p}}} \tag{10}$$

Here, V_{Tp} and V_{Tn} are the threshold voltages of the PMOS and NMOS transistors in that order; μ_n and μ_p are the average mobility of electrons and holes respectively, and $(W/L)_n/(W/L)_p$ is the ratio of the aspect ratio of the NMOS transistor to the aspect ratio of the PMOS transistor [27].

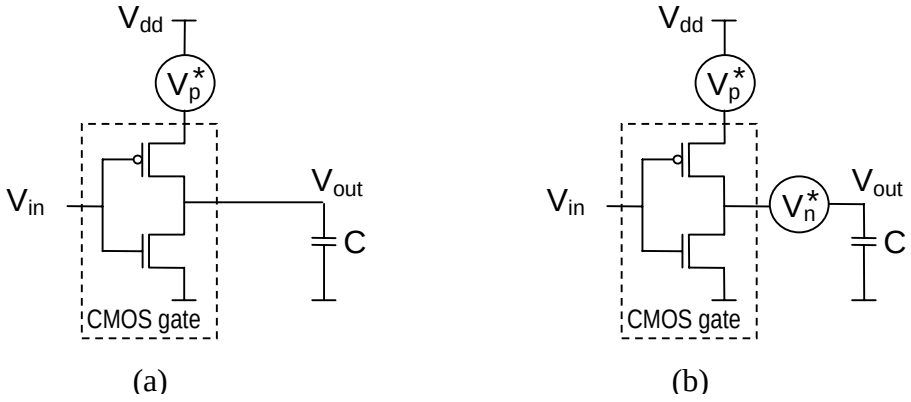

Figure 7. Couplings of the power supply noise to the CMOS (inverter) gate: (a)Power supply noise only (b) Power supply noise in conjuction with output-coupled thermal noise

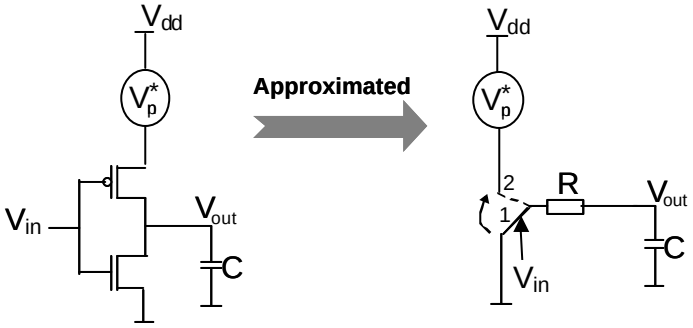

Figure 8. The approximation to a CMOS inverter coupled with power supply noise

5.2 Analytical Modeling of the Probability Parameter (p) of a PCMOS Inverter with Power Supply Noise Coupling

In this section, we develop an analytical model characterizing the probabilistic behavior of a CMOS inverter. We assume that the power supply voltage has a Gaussian distribution with an RMS value in the order of a few hundred milivolts. This assumption is based on the stochastic modeling of power supply noise presented in [20], where it is concluded that power supply noise can be modeled as a random signal with a Gaussian distribution, especially for large chips having large number of cells/blocks. In the sequel, we refer to the RMS value of power supply noise as σ_p.

Our analytical model considers two cases of power supply noise coupling. In the first case, the power supply noise, denoted as $V_p{}^*$, is the only noise source coupled to the inverter as shown in Figure 7(a). Figure 7(b), on the other hand, illustrates the second case where the power supply noise, is coupled to the inverter in conjuction with the output-coupled (thermal) noise source, denoted as $V_n{}^*$.

5.2.1 *Analytical Modeling of the Probability Parameter (p) of a* PCMOS *Inverter Coupled with Only Power Supply Noise.* In the case that the CMOS inverter is coupled with only the power supply noise (as shown in Figure 7(a)), the approximation illustrated in Figure 8 is utilized to simplify the analysis. Similar to the case of inverter coupled with thermal noise, the inverter is approximated as an ideal switch.

Referring to Figure 8, if the power supply noise is not present, and when $V_{in} = V_{dd}$, the ideal switch will

be in position 1, that is, the NMOS transistor will be ON and the PMOS transistor will be OFF. Similarly, if the power supply noise is not present, and $V_{in} = 0$, the ideal switch will be in position 2, that is the PMOS transistor will be ON, and the NMOS transistor will be OFF. However, due to the power supply noise, the PMOS transistor may become ON, even in the case that $V_{in} = V_{dd}$ and it may become OFF, even in the case that $V_{in} = 0$.

In the case that $V_{in} = 0$, the gate to source voltage (V_{gsp}) of the PMOS transistor is

$$V_{gsp} = V_{gp} - V_{sp} = 0 - (V_{dd} + {V_p}^*) = -V_{dd} - {V_p}^* \tag{11}$$

Since V_{gsp} is a linear combination of the input signal V_{gp} (constant) and the random signal ${V_p}^*$, V_{gsp} is also a random signal having a Gaussian distribution with an RMS value of σ_p [21]. If $|V_{gsp}|$ drops below the threshold voltage of the PMOS transistor ($|V_{Tp}|$), the PMOS transistor becomes OFF causing the output node to become a high impedance node. In this case, the output node may have a binary value of 0 or 1. We assume that the probability of the output voltage (V_{out}) being 0 or 1 is $\frac{1}{2}$ for both cases. The probability of $|V_{gsp}|$ being smaller than $|V_{Tp}|$ can be found using (12).

$$Pr\left(|V_{gsp}| < |V_{Tp}|\right) = \frac{1}{2} - \frac{1}{2} erf\left(\frac{V_{dd} - |V_{Tp}|}{\sqrt{2}\sigma_p}\right) \tag{12}$$

If $|V_{gsp}|$ is greater than ($|V_{Tp}|$), then the ideal switch in Figure 8 is in position 2, and the noise source V_p^* will constitute an offset on V_{dd}. V_{out} is described with the Gaussian distribution (corresponding to the curve on the right in Figure 6), where the RMS value of the Gaussian distribution is σ_p.

Thus, for an inverter coupled only with power supply noise, in the case that $V_{in} = 0$, the probability of error (the probability of 1 being interpreted as 0) is described by

$$e_{10} = Pr(|V_{gsp}| \geq |V_{Tp}|) \cdot \left(\frac{1}{2} - \frac{1}{2} erf\left(\frac{V_m}{\sqrt{2}\sigma_p}\right)\right) + Pr(|V_{gsp}| < |V_{Tp}|) \cdot \frac{1}{2} \tag{13}$$

Referring to Figure 8, in the case that $V_{in} = V_{dd}$, the gate to source voltage (V_{gsp}) of the PMOS transistor is described by

$$V_{gsp} = V_{gp} - V_{sp} = V_{dd} - (V_{dd} + {V_p}^*) = -{V_p}^* \tag{14}$$

The PMOS transistor may become ON, that is the ideal switch in Figure 8 might erroneously switch to position 2, if $|V_{gsp}|$ is greater than the threshold voltage ($|V_{Tp}|$) of the PMOS transistor. However, not every value of $|V_{gsp}|$ can cause an incorrect transition at the output from binary 0 to 1. We refer to the value of $|V_{gsp}|$ above which we observe incorrect transitions at the output as V_{mp} (a positive real number). Below, we will derive V_{mp} using Schichman-Hodges MOSFET model [7].

Referring to Figure 9, which shows the input and output voltages of an inverter with an additional DC voltage of V_{gsp} on its power supply, in the case $V_{in} = V_{dd}$, and $V_{out} = \frac{V_{dd}}{2}$, the gate to source and drain to source voltages of the PMOS and NMOS transistors, V_{gsp}, V_{dsp}, V_{gsn} and V_{dsn}, respectively, are described below by equations 15 and 16.

$$\begin{aligned} V_{gsp} &= -{V_p}^* \\ V_{dsp} &= -\tfrac{V_{dd}}{2} - V_p \end{aligned} \tag{15}$$

$$\begin{aligned} V_{gsn} &= V_{dd} \\ V_{dsn} &= \tfrac{V_{dd}}{2} \end{aligned} \tag{16}$$

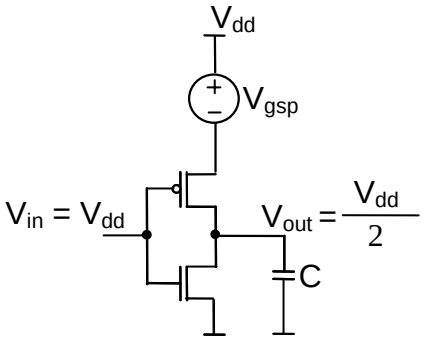

Figure 9. The input and output voltages of the inverter in the case that there is a DC voltage of V_{gsp} on the power supply line

Using Schichman-Hodges MOSFET model, the drain currents of the PMOS and NMOS transistors are described by

$$\begin{aligned} I_{dp} &= \mu_p \left(\tfrac{W}{L}\right)_p C_{ox} \tfrac{(V_{mp}-V_{Tp})^2}{2} \\ I_{dn} &= \mu_n \left(\tfrac{W}{L}\right)_n C_{ox} \left(\tfrac{3}{4}V_{dd} - V_{Tn}\right) \tfrac{V_{dd}}{2} \end{aligned} \tag{17}$$

Solving for V_{mp} in $I_{dp} = I_{dn}$, we find that

$$V_{mp} = \sqrt{(\mu_n/\mu_p)\,\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} V_{dd}\left(\frac{3V_{dd}}{4} - V_{Tn}\right)} + |V_{Tp}| \tag{18}$$

Using equation (18) and through HSpice simulations, we have found that V_{mp} is approximately equal to V_{dd}.

Using (14), we find that the following condition for ${V_p}^*$ should hold in order that an error occurs at the output

$${V_p}^* \geq V_{mp} \tag{19}$$

Hence, the probability of an error occurring at the output due to power supply noise in the case of the inverter input being V_{dd} is identical to the probability of ${V_p}^*$ being greater than V_{mp}, wherein ${V_p}^*$ is a random variable with a Gaussian distribution of RMS value σ_p. Thus, the probability of an erroneous switching from 0 to 1 (e_{01}) at the output of the CMOS inverter is

$$e_{01} = \frac{1}{2} - \frac{1}{2} erf\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) \tag{20}$$

Hence, from (20), (13) and (8) the probability of being correct in the case of power supply noise coupling becomes

$$p = \frac{1}{2} + \frac{1}{4} erf\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) + \frac{1}{8} erf\left(\frac{V_{dd}-V_m}{\sqrt{2}\sigma_p}\right) + \frac{1}{8} erf\left(\frac{V_{dd}-V_m}{\sqrt{2}\sigma_p}\right) \cdot erf\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) \tag{21}$$

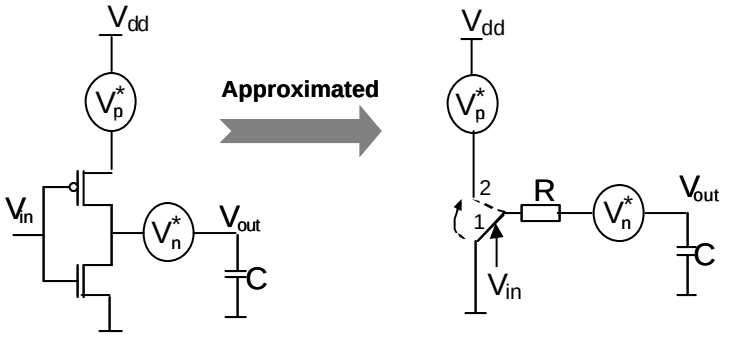

Figure 10. The approximation for a CMOS inverter with power supply noise coupled to its power supply line and thermal noise coupled to its output

5.2.2 *Analytical Modeling of the Probability Parameter (p) of a* PCMOS *Inverter Coupled with Power Supply Noise plus Thermal Noise.* In this section, we consider a CMOS inverter whose probabilistic behavior is induced by power supply noise coupled to its power supply line and thermal noise coupled to its output. The CMOS inverter is replaced by the simplified model shown in Figure 10 to derive the analytical model. Similar to the case of the inverter being coupled only with power supply noise, we consider the cases of $V_{in} = 0$ or $V_{in} = V_{dd}$.

Referring to Figure 10, in the case that $V_{in} = 0$, V_{gsp} is described by (11). As explained in Section 5.2.1, V_{gsp} is a random variable having a Gaussian distribution with an RMS value of σ_p. If $|V_{gsp}|$ drops below $|V_{Tp}|$, the PMOS transistor becomes OFF, and the output node becomes a high impedance node. We assume that the binary value of V_{out} is 0 or 1 with probability $\frac{1}{2}$. The probability of $|V_{gsp}|$ being smaller than $|V_{Tp}|$ was described by (12).

In the case of $V_{in} = 0$ and $|V_{gsp}| > |V_{Tp}|$, the ideal switch in Figure 10 will be in position 2, and the noise sources V_p^* and V_n^* will be additive, leading to an equivalent noise with a Gaussian distribution [13]. We note that the power supply and thermal noise sources are derived from statistically independent Gaussian processes. The RMS value of this equivalent noise is denoted by σ_a and calculated as follows

$$\sigma_a = \sqrt{\sigma_p^2 + \sigma^2} \tag{22}$$

Thus, for an inverter coupled with power supply noise in conjuction with the output-coupled thermal noise, when $V_{in} = 0$, the probability of 1 being treated as 0 (e_{10}) is described by

$$e_{10} = Pr(|V_{gsp}| \geq |V_{Tp}|) \cdot \left(\frac{1}{2} - \frac{1}{2} erf\left(\frac{V_m}{\sqrt{2}\sigma_a}\right)\right) + Pr(|V_{gsp}| < |V_{Tp}|) \cdot \frac{1}{2} \tag{23}$$

Referring to Figure 10, in the case when $V_{in} = V_{dd}$, the PMOS transistor may become ON because of the power supply noise. In Section 5.2.1 we derived V_{mp}, the value of V_{gsp} above which we observe incorrect transitions at the output when $V_{in} = V_{dd}$. The probability of the PMOS transistor becoming ON to propagate the errors due to the power supply noise to the output is described by

$$Pr(|V_{gsp}| \geq V_{mp}) = \frac{1}{2} - \frac{1}{2} erf\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) \tag{24}$$

In the case when $|V_{gsp}| < V_{mp}$, we assume that the only noise source affecting the output is the thermal noise source. In the case when $|V_{gsp}| > V_{mp}$, the noise sources V_p^* and V_n^* are additive leading to an equivalent

Gaussian noise source with RMS value of σ_a (described by (22)). Then, the probability of an incorrect switching from 0 to 1 (e_{01}) is described as follows

$$e_{01} = Pr(|V_{gsp}| < V_{mp}) \cdot \left(\frac{1}{2} - \frac{1}{2}erf\left(\frac{V_m}{\sqrt{2}\sigma}\right)\right) + Pr(|V_{gsp}| \geq V_{mp}) \cdot \left(\frac{1}{2} - \frac{1}{2}erf\left(\frac{V_m}{\sqrt{2}\sigma_a}\right)\right) \tag{25}$$

Using (25), (23) and (8) the probability of being correct for a CMOS inverter with power supply noise coupled to its power supply line plus the thermal noise source coupled to its output becomes

$$\begin{aligned} p = \; & \tfrac{1}{2} + \tfrac{1}{8}erf\left(\tfrac{V_m}{\sqrt{2}\sigma}\right) + \tfrac{1}{8}erf\left(\tfrac{V_m}{\sqrt{2}\sigma_a}\right) + \tfrac{1}{8}erf\left(\tfrac{V_{dd}-V_m}{\sqrt{2}\sigma_a}\right) + \tfrac{1}{8}erf\left(\tfrac{V_{mp}}{\sqrt{2}\sigma_p}\right) \cdot erf\left(\tfrac{V_m}{\sqrt{2}\sigma}\right) - \\ & \tfrac{1}{8}erf\left(\tfrac{V_{mp}}{\sqrt{2}\sigma_p}\right) \cdot erf\left(\tfrac{V_m}{\sqrt{2}\sigma_a}\right) + \tfrac{1}{8}erf\left(\tfrac{V_{mp}}{\sqrt{2}\sigma_p}\right) \cdot erf\left(\tfrac{V_{dd}-V_m}{\sqrt{2}\sigma_a}\right) \end{aligned} \tag{26}$$

5.3 Analytical Modeling of the E-p Relationship of a PCMOS Inverter

In the previous two sections, we provided analytical models characterizing the probability parameter (p) of a CMOS inverter coupled with thermal noise and/or power supply noise. In this section, we will first provide analytical models characterizing the (dynamic) energy consumed per one switching step (E) of CMOS inverter. Following this, we will depict the relationship between p and E.

5.3.1 *Modeling the Energy Consumed by a* CMOS *Inverter per Switching.* The main components of dynamic energy consumption of a digital circuit are switching energy consumption (E_{sw}) and short-circuit energy consumption (E_{sc}). We model the switching energy consumption using

$$E_{sw} = \frac{1}{2}CV_{dd}^2 \tag{27}$$

which describes the energy consumed to charge (from 0 to V_{dd}) or discharge (from V_{dd} to 0) a capacitive load C.

The energy consumption of each approximated circuit in Figures 5, 8 and 10 is described by (27). In this section, we will consider only the switching energy consumption ($E \approx E_{sw}$) and will use (27) to derive the E-p relationship of a CMOS inverter. However, the short-circuit energy consumption of the inverter can constitute up to 20% of dynamic energy consumption of the inverter [1] and should also be taken into account in the analytical model. In Section 7, we will present an improved analytical model characterizing the E-p relationship, wherein the short-circuit energy consumption of the CMOS inverter is also accounted for in modeling E.

5.3.2 *E-p Relationship for a* PCMOS *Inverter.* In this section, we first present a generalized form of the E-p relationship. Following this, we provide the E-p relationship of a CMOS inverter that is symmetric and coupled with thermal noise.

It is evident from (9), (21) and (26) that p is a function of V_{dd}. It is also seen that this function is dependent on the type of the noise coupling. We denote this function by h_i, where i is an arbitrary integer associated with the type of coupling. For example, if we choose i to be 1 in the case that thermal noise is coupled to the input and i to be 2 in the case of output-coupled thermal noise, then $p = h_1(V_{dd}) = h_2(V_{dd})$ and $h_1(V_{dd})$ is

$$h_1(V_{dd}) = \frac{1}{2} + \frac{1}{4}erf\left(\frac{V_m}{\sqrt{2}\sigma}\right) + \frac{1}{4}erf\left(\frac{V_{dd}-V_m}{\sqrt{2}\sigma}\right) \tag{28}$$

where V_m is described by (10).

From (27), the generalized E-p relationship is described as follows

$$E = \frac{1}{2} C \left[h_i^{-1}(p) \right]^2 \tag{29}$$

where $h_i^{-1}(x)$ denotes the inverse of the function $h_i(x)$.

If the transistors of the inverter are symmetrical (with equal threshold voltages, and satisfying the condition $(\mu_n/\mu_p) = (W/L)_p / (W/L)_n$), then the following equations describe the E-p relationship for two instances of coupling: In the instance that thermal noise is coupled to the input or to the output of a symmetric inverter, E-p relationship is

$$E = 4C\sigma^2 \left[inverf(2p-1) \right]^2 \tag{30}$$

where *inverf* is the inverse of the error function [26].

The expression in (30) shows that E increases with p and this increase in E is approximately exponential in p, since $inverf(x)$ function can be expressed as a series summation of powers of x^2 [26] (similar to $\exp(x^2)$). Similarly, with an increasing RMS value of noise for a fixed probability value p, the energy consumed to produce a bit increases. The increase in E is quadratic with respect to the increase in RMS value of noise.

6. VALIDATION OF THE ANALYTICAL RESULTS

To validate our analytical results, we performed circuit simulations in HSpice for CMOS inverters realized in AMI 0.5μm and TSMC 0.25μm processes. Table 1 summarizes the simulation parameters. As seen in the table, the parameters that are varied are the supply voltage (V_{dd}), RMS value of the thermal noise (σ_n), and RMS value of the power supply noise (σ_p). The load capacitance value (C) corresponds to a load due to a fanout of four (which is a typical load value), leading to a value of 60fF and 28fF for AMI 0.5μm and TSMC 0.25μm, respectively.

In this section, we primarily present the analytical and simulation results for a CMOS inverter realized in TSMC 0.25μm process. The results for an inverter realized in AMI 0.5μm process show similar trends.

Table 1. Simulation Parameters

Technology		AMI **0.5μm**	TSMC **0.25μm**
Inverter fan-out		4	4
Load capacitance		60fF	28fF
Nominal Vdd (V)		5	2.5
Transistor size	**(W/L)$_{pmos}$**	15u/0.6u	2u/0.3u
	(W/L)$_{nmos}$	6u/0.6u	0.8u/0.3u
Vdd (V)		0.5-5	0.5-2.5
σ (V)		0.2-0.8	0.2-0.8
σ_p (V)		0.2-0.8	0.2-0.8
Input rise and fall time		0.2ns	0.2ns

In our simulations, noise is inserted into the HSpice netlists in the form of a PWL (PieceWise Linear) voltage source. The data points of the PWL source are from a Gaussian distribution of random numbers generated by Matlab. In Figure 11, we show the rise and fall times of the noise pulse. As shown in the figure, t_{nr} denotes the rise time of the noise pulse, t_{nf} denotes the fall time of the noise pulse, and they are identical to each other ($t_{nr} = t_{nf}$), and t_{nc} denotes the length of the time during which the noise voltage level is kept constant. In addition, t_{sn} denotes sampling period of the noise, and is equal to the sum of the t_{nf} (or t_{nr}) and t_{nc}.

In Section 5.1, we stated that noise is sampled at the beginning of the switching, and held at the sampled value during switching. Furthermore, the sampling period of the noise is larger than the switching time (T_s)

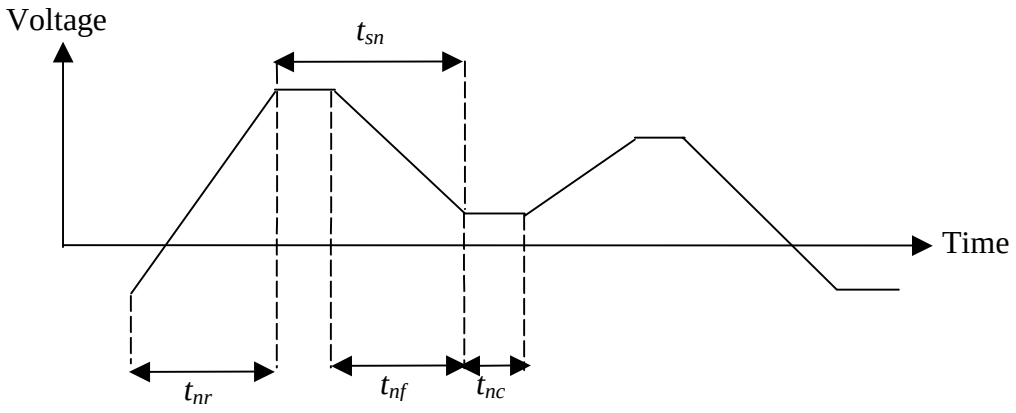

Figure 11. The noise pulse and its rise and fall times

of the inverter. We refer to this method of sampling and holding the noise voltage as the noise voltage being *latched*. On the other hand, in the typical way of generating a noise source for transient response circuit simulations [5], referring to Figure 11, t_{nc} is identical to zero. We refer to this method of generating noise as the noise being *non-latched*. In this section, our results are based on the case that noise is latched. In Section 8, we will consider the case that noise is non-latched, and we will illustrate the impact of not latching the noise on the probabilistic behavior of the CMOS inverter. We note that latching the noise is not the same as the digital latching.

In this section, the period with which V_{out} is sampled, denoted t_{so}, is equal to the noise sampling period, t_{sn}.

In simulations, p is found by calculating the ratio of the number of the correct simulation points to the ratio of the total number of simulation points. The correctness is identified by comparing the simulation results (for V_{out}) in the case when there is noise coupling to the case when there is not any noise coupling. Moreover, E is determined through measuring the total current drawn from the supply voltage of the inverter when the input of the inverter is connected to a pulse signal. The last row of Table 1 shows the value of the rise and fall times of the input pulse. Note that, an inverter also consumes short-circuit energy during a switching. In the simulations, since the total current drawn from the supply voltage is measured, the resulting energy consumption also includes the short-circuit energy consumption. We also note that we only measure the energy consumed by a CMOS inverter during one switching step, that is, when its output changes (switches) from 0 to V_{dd} or vice versa. Later in Section 9, we will show the impact of the spurious switchings resulting from noise on the energy consumption of a CMOS inverter.

Below, we first present the analytical and simulation results for the E-p relationship of a CMOS inverter that is coupled with thermal noise at its input or output. Following this, we compare the analytical and simulation results for the E-p relationship of a CMOS inverter coupled with power supply noise. Then, we depict the analytical and simulation results for the E-p relationship of a CMOS inverter coupled with power supply noise and thermal noise.

6.1 E-p Relationship for a CMOS Inverter Coupled with Thermal Noise

In Figure 12, we depict the E-p relationship of CMOS inverters realized using a TSMC 0.25μm and an AMI 0.5μm technology, and coupled with thermal noise at their outputs or inputs. The figure shows the E-p relationship estimated using HSpice simulations as well as the E-p relationship resulting from the analytical

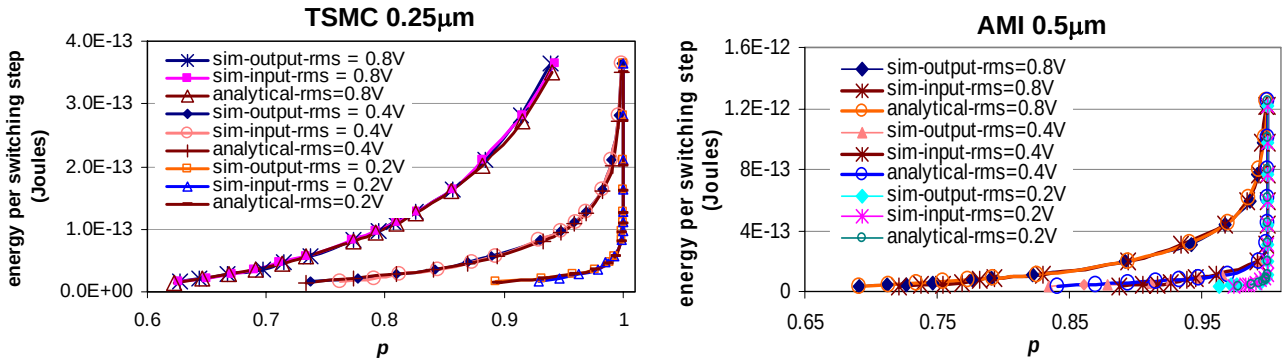

Figure 12. E-p relationship for an inverter with thermal noise coupled to its input or output

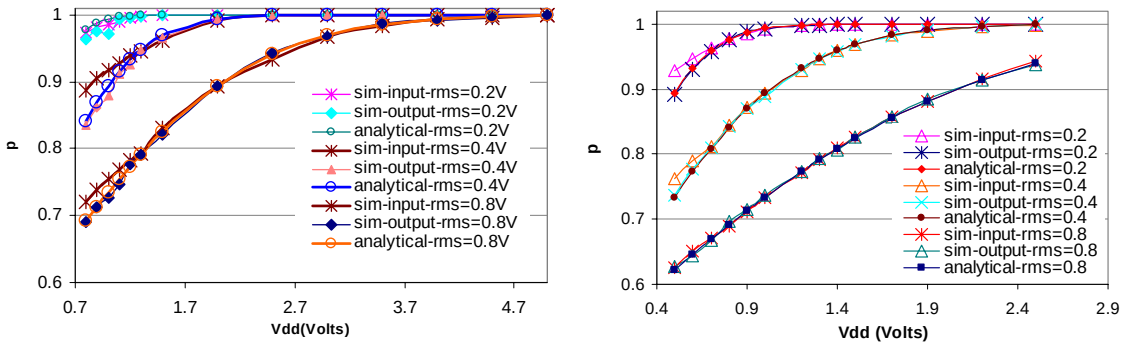

Figure 13. The change in p with respect to V_{dd} of a CMOS inverter coupled with thermal noise at its input or output

model. The two parameters that we vary are the noise RMS value, σ, and the operating supply voltage, V_{dd}. In particular, for each value of RMS value of noise, we calculate p at different values of V_{dd} through the analytical model (described by (9)), and through circuit simulations in HSpice. In the figure, sim-output-rms denotes the simulation results in the case of the output-coupled thermal noise. Similarly, sim-input-rms denotes the simulation results in the case of input-coupled thermal noise. We estimate the energy consumed per switching of a CMOS inverter using the analytical model (described by (27)) as well as through the circuit simulations. As shown in Figure 12, given a fixed amount of available noise, the energy needed to produce a single bit increases with p. Furthermore, with increasing RMS for a fixed probability value p, the energy consumed to produce a bit increases. Analytical and simulation results agree in terms of these two trends observed for the energy consumed per switching. In addition, it is seen in Figure 12 that the simulation results for the cases of input- and output-coupled noise are very close to each other, showing the validity of the analytical model described by (29). We note that our analytical model for instances of output-coupled and input-coupled noise are the same.

As seen in Figure 12, the difference between the results of the analytical model and the simulations is negligible. Since our analytical model consists of two aspects, the first modeling p and the second modeling E, we also investigate the accuracy of these two components of the analytical model separately. In Figure 13, we depict p versus V_{dd} at different values of noise RMS value. Figure 13 shows that analytical and simulation results for p follow each other very closely (the difference is 1.04% in the average). Figure 14 shows the energy estimation results of the analytical model and the simulations with respect to V_{dd}. The difference between the

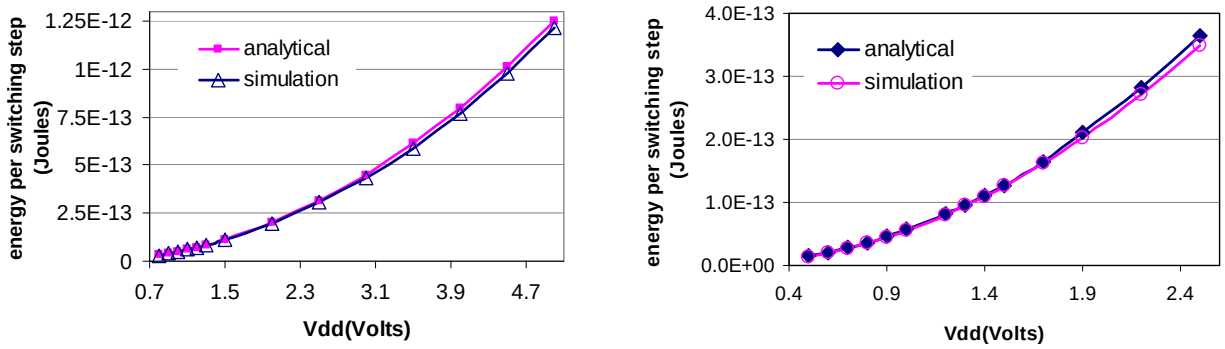

Figure 14. Energy results for the analytical model and the simulations

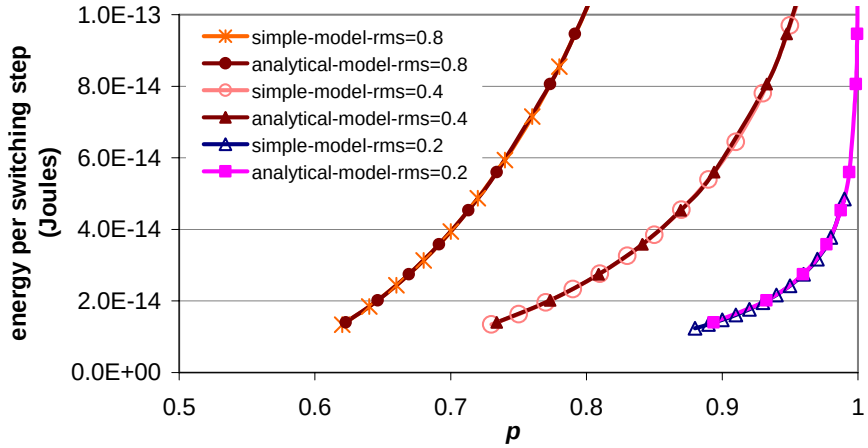

Figure 15. Comparison of the simple analytical model (30) with the analytical model described by (29)

results of the analytical model and simulations is 2.82% in the average. Hence, our analytical model produces reasonably accurate estimates for p as well as E.

Figure 13 also shows that for a CMOS inverter coupled with thermal noise at its input, and for noise RMS values of 0.2V and 0.4V, the deviation of the analytically found p from the p found through simulations increases as V_{dd} decreases. For example, for the 0.25μm inverter, when the RMS value of noise is 0.2V, the deviation becomes noticeable at $V_{dd} = 0.7$V and increases as V_{dd} decreases below 0.7V. This trend results due to the fact that, as V_{dd} decreases, the propagation delay of the CMOS inverter increases resulting in the noise being low-pass filtered. We will revisit this issue in Section 8, where we discuss the impact of the equivalent noise bandwidth and the propagation delay of the inverter gate on the probabilistic behavior of a CMOS inverter.

In Section 5.3.2, we presented a simple expression modeling the E-p relationship of a symmetric inverter in (30). In Figure 15, we provide a comparison of the E-p relationship (for a TSMC 0.25μm inverter) obtained using (30) with the E-p relationship obtained using (29) at different values of noise RMS. In the figure, simple-model refers to the analytical model described by (30). The figure shows that the simple analytical model agrees very closely with the analytical model described by (29). The reason for the strong agreement between the two models is because that our TSMC 0.25μm inverter has a midpoint voltage, V_m, that is very close to V_{dd} /2.

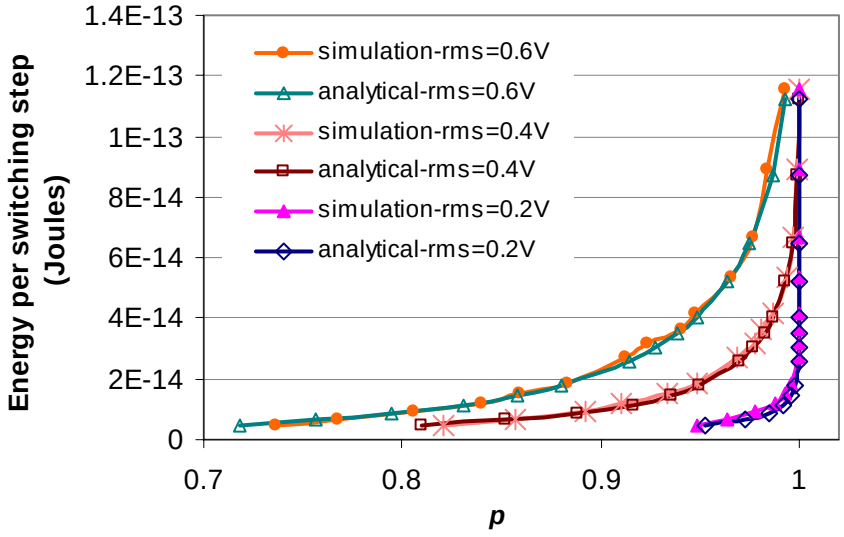

Figure 16. The E-p relationship in case of power supply noise coupling

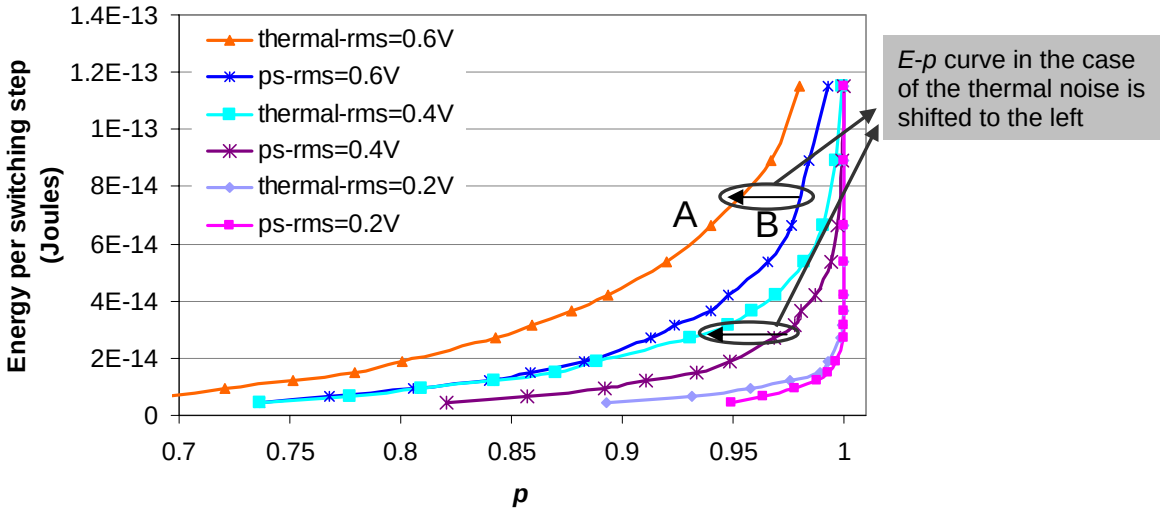

Figure 17. The comparison of the E-p relationships in the instances of power supply noise coupling and output coupling of thermal noise

6.2 E-p Relationship for a CMOS Inverter Coupled with Power Supply Noise

Figure 16 shows the E-p relationship of a CMOS inverter coupled only with the power supply noise. We vary the supply voltage of the inverter and the RMS value of the power supply noise coupled to the inverter. Similar to the case of the thermal noise coupled to the input or the output of the CMOS inverter, given a fixed amount of available noise, the energy needed to produce a single bit increases with p. In addition, with increasing RMS value of noise for a fixed probability value p, the energy consumed to produce a bit is increasing. As seen in

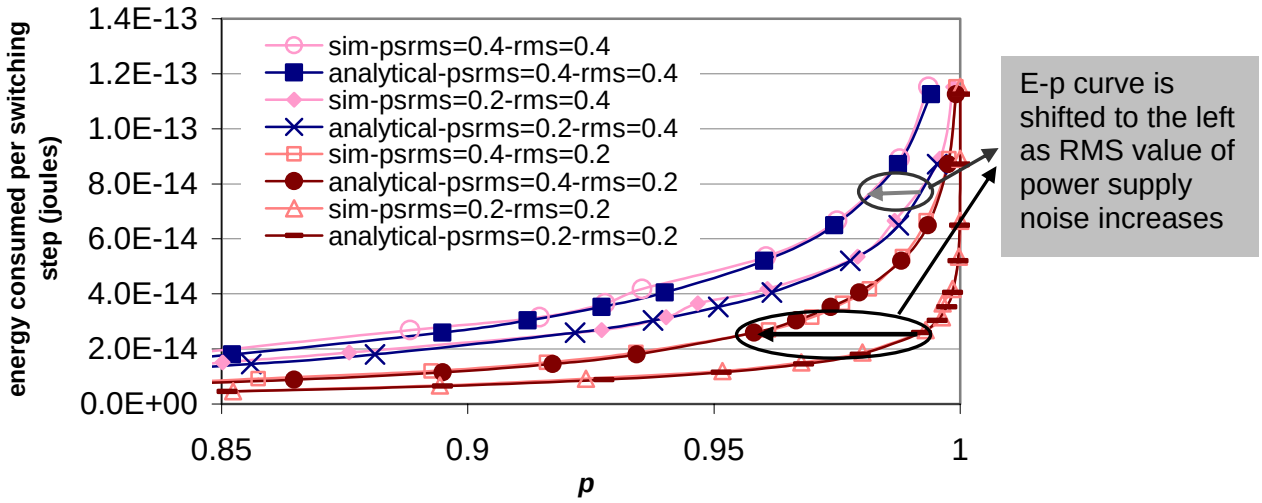

Figure 18. The *E-p* relationship for a CMOS inverter with power supply noise coupled to its power supply line and thermal noise coupled to its output

the figure, the difference between the results of the analytical model and the simulations is negligible.

Figure 17 shows a comparison of the *E-p* relationships of a CMOS inverter in the instances of output-coupled thermal noise and power supply noise coupling. In the figure, thermal-rms denotes the rms value of the thermal noise, and ps-rms denotes the rms value of the power supply noise. The figure depicts that at a fixed value of E, output-coupled thermal noise induces a lower value of p when compared to power supply noise with the same magnitude. Hence, output-coupled thermal noise is more effective in generating a specific value of p, that is the required noise RMS value in the case of the output-coupled thermal noise is smaller. The higher value of p in the instance of the power supply noise coupling results due to the fact that power supply noise induces less errors when the input voltage of the inverter is V_{dd}.

6.3 *E-p* Relationship for a CMOS Inverter Coupled with Power Supply Noise plus Thermal Noise

Figure 18 shows the *E-p* relationship for a CMOS inverter in the instance that it is coupled with power supply noise at its power supply line and thermal noise at its output. In the figure, both the RMS value of thermal noise and the RMS value of power supply noise are varied. Similar to the three previous coupling instances, given a fixed amount of available noise, the energy needed to produce a single bit increases with p. In addition, with increasing noise RMS value for a fixed probability value p, the energy consumed to produce a bit increases. In Figure 18, from left to right, the first four curves represent the *E-p* relationship of an inverter coupled with power supply noise in conjuction with output-coupled thermal noise, wherein the RMS value of thermal noise is 0.4V. In the case of the next four curves in the figure, the RMS value of thermal noise is 0.2V. These curves depict that the *E-p* curve is shifted to the left as the RMS value of power supply noise increases. However, the impact of varying the RMS value of the power supply noise becomes less significant as the RMS value of the output-coupled thermal noise increases. For example, when the RMS value of thermal noise is 0.2V, increasing the RMS value of power supply noise from 0.2V to 0.4V shifts the *E-p* curve through the distance shown by the black arrow, whereas when the RMS value of thermal noise is 0.4V, the *E-p* curve is shifted by a smaller distance shown by the gray arrow. This trend occurs because the proportion of power supply noise decreases as the RMS value of thermal noise increases.

Figure 19 shows the *E-p* relationship of a CMOS inverter coupled with thermal noise of varying RMS values

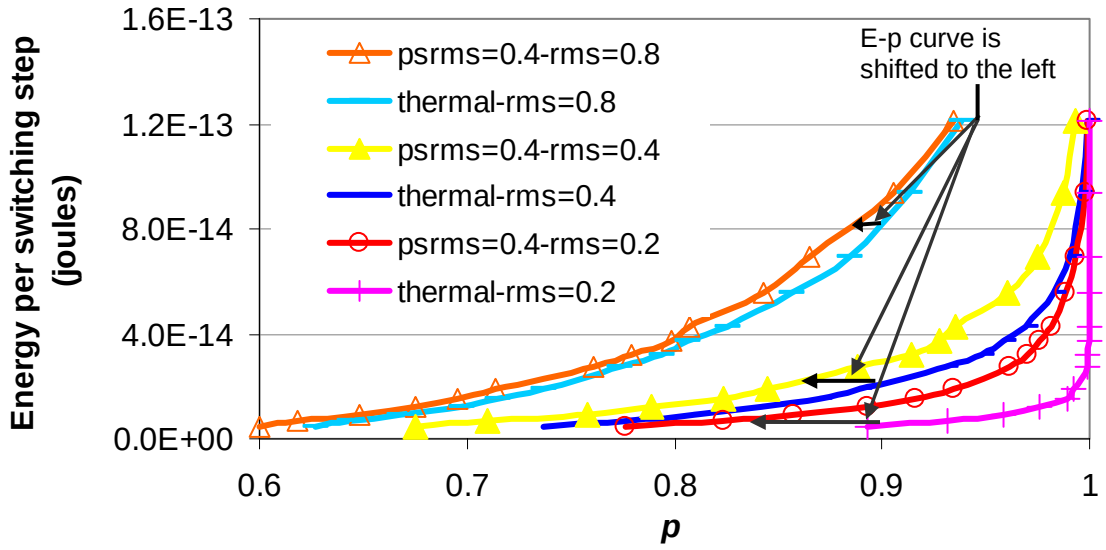

Figure 19. Comparison of E-p relationships for a CMOS inverter for two cases: (1) inverter is coupled with power supply noise and thermal noise, (2) inverter is coupled with only thermal noise

(0.2V, 0.4V, and 0.8V) at its output and power supply noise with RMS value of 0.4V. In addition, the figure depicts the E-p relationship of the same CMOS inverter when it is coupled only with thermal noise. The figure shows that when power supply noise is coupled in addition to the thermal noise, the E-p curve is shifted to the left. We also observe that, the distance by which the E-p curve is shifted to the left increases as the RMS value of the thermal noise decreases. This results from the increasing effect of the power supply noise on p.

6.4 Summary of the Results

In this section, we have validated our analytical models for the E-p relationship in four cases of noise coupling: (1) thermal noise coupled at the input (2) thermal noise coupled at the output (3) power supply noise (4) power supply noise in conjuction with the thermal noise coupled at the output. We have found that given a fixed amount of available noise, the energy needed to produce a single bit increases with p. The analytical model and simulation results have shown that this increase is approximately exponential. We also observed that with increasing RMS for a fixed probability value p, the energy consumed to produce a bit increases. Our analytical results and simulation results have depicted that the increase in E with increasing RMS is quadratic.

We have observed that our analytical models produce accurate results for all of the four instances of coupling. However, in the case of the input-coupled noise, we have observed that the analytically calculated value of p is smaller than the value of p found through simulations at low values of the supply voltage. The difference between the two occurs due to the increased propagation delay of the inverter at low values of V_{dd}. We will revisit this issue in Section 8.

In our analytical models, we have only considered the switching energy component of the energy consumption of the inverter. In Section 7, we will consider the short-circuit energy consumption, since the short-circuit energy consumption can constitute upto 20% of the dynamic energy consumption [1].

7. AN IMPROVED ENERGY MODEL

In Section 6, we obtained the E-p relationship of a CMOS inverter coupled with thermal noise and/or power supply noise, and compared the analytically estimated E-p relationship with the E-p relationship found through the simulations. We observed that there is a negligible difference between the analytically estimated E-p relationship and the E-p relationship found through HSpice simulations. Furthermore, we observed that the negligible difference between the results of the analytical model and the simulations is caused by not only the accuracy of the analytical model in estimating p but also the accuracy of the analytical model in estimating the energy. In this section, first we consider a different scenario. In this scenario, the energy estimation of the analytical model is not as accurate as it was in Section 6, because the short-circuit energy dissipation of the inverter is more prominent. Second, we provide a sketch of an improved energy estimation model wherein we include the short-circuit energy dissipation of the CMOS inverter. The details of our short-circuit energy estimation model can be found in [11].

7.1 The Accuracy of the Analytical Energy Estimation

In Section 6, the energy estimation results found by the analytical model and by the simulations differed only by 2.14%. However, when the simulations are repeated with the parameters shown in Table 2, wherein the rise and fall times of the input signal are higher, we observe that the energy estimation results obtained using our analytical model deviate from the energy estimates found through the simulations. The simulation parameters in Table 2 are estimated based on the results of the simulations and the physical measurements performed on an inverter designed, extracted and fabricated in a TSMC $0.25\mu m$ technology. For example, the load capacitance, which is 130fF (as shown in Table 2) corresponds to the sum of the drain capacitances of the inverter transistors and the input capacitance of the output driver (which is implemented to drive high capacitive loads that are incurred during the physical measurements). As we will show below, the deviation between the energy estimates from the analytical model and from the simulations is caused by the increase in the short-circuit energy dissipation.

Table 2. Simulation parameters for the fabricated inverter

Technology		TSMC **0.25μm**
Inverter fan-out		7
Load capacitance		130fF
Nominal Vdd (V)		2.5
Inverter transistor sizes	**(W/L)**$_{pmos}$	6.72u/0.24u
	(W/L)$_{nmos}$	3.36u/0.24u
Vdd (V)		1.5-2.5
σ **(V)**		0.2-0.8
σ_p **(V)**		0.2-0.8
Input rise- and fall-time		2ns

Figure 20 shows the E-p relationship of a CMOS inverter coupled by thermal noise at its input. The simulation and analytical results are obtained using the parameters shown in Table 2. As seen in the figure, there is a significant difference between the simulation and the analytical results. To eliminate the possibility of this significant difference being caused by the deterioration in the estimation of p by the analytical model, in Figure 21 we show a comparison of the analytically estimated p and the p value obtained through the simulations. Figure 21 shows that analytically estimated p and the p value found through the simulations are very close to each other. Hence, the difference between the analytically estimated E-p relationship and the E-p relationship found through the simulations is caused by the deviation in E.

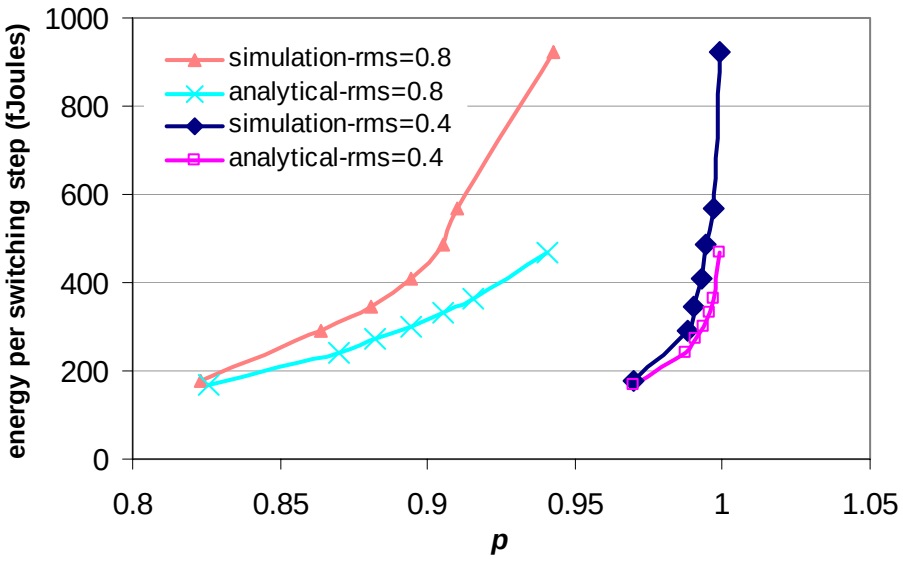

Figure 20. E-p relationship of the CMOS inverter with the parameters shown in Table 2 in case when the inverter is coupled with thermal noise at its input

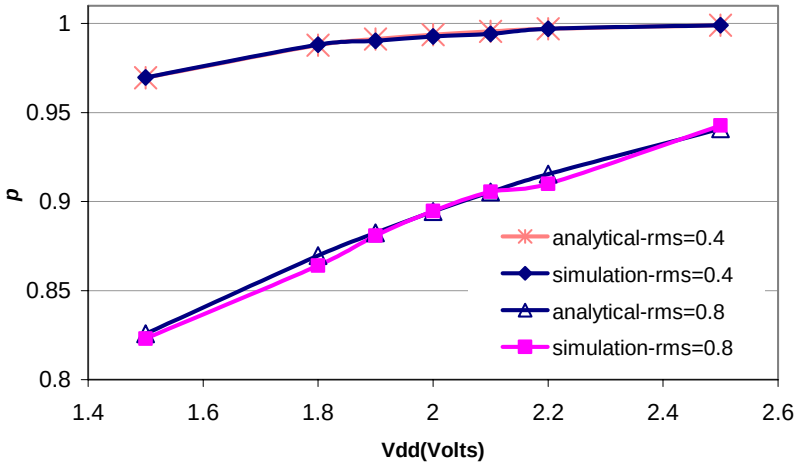

Figure 21. The change in p with respect to V_{dd} for the CMOS inverter with the E-p relationship shown in Figure 20

We note that, in the circuit simulations, we measure the total energy consumption incurred during one switching of the inverter. Hence, a simulation result is comprised of the switching energy consumption and the short-circuit energy dissipation. To identify the reason for the difference between the analytically estimated E and the E found through the simulations, we measure the switching energy consumption of the inverter seperately through simulations. A comparison of the switching energy consumption found through simulations and the switching energy consumption obtained analytically is illustrated in Figure 22.

As shown in Figure 22, there is a minor difference between the analytically estimated switching energy and

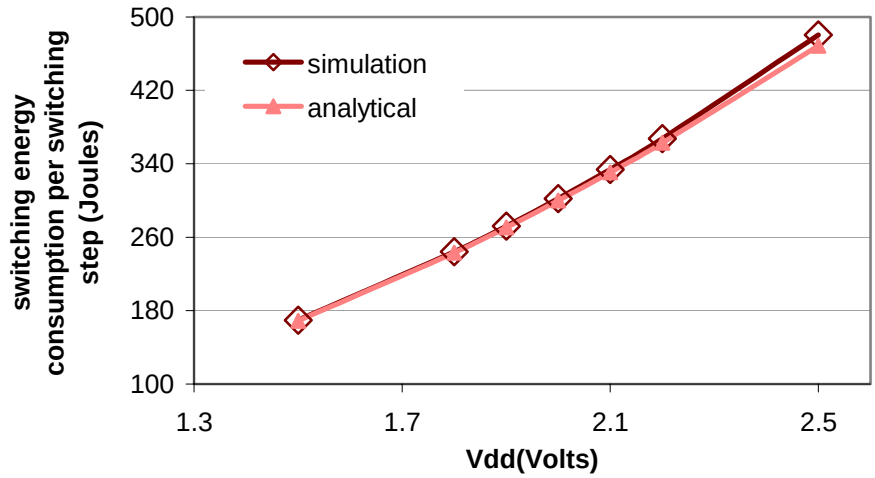

Figure 22. The comparison of the analytically estimated swithing energy consumption and the corresponding simulation result for the CMOS inverter with the parameters shown in Table 2

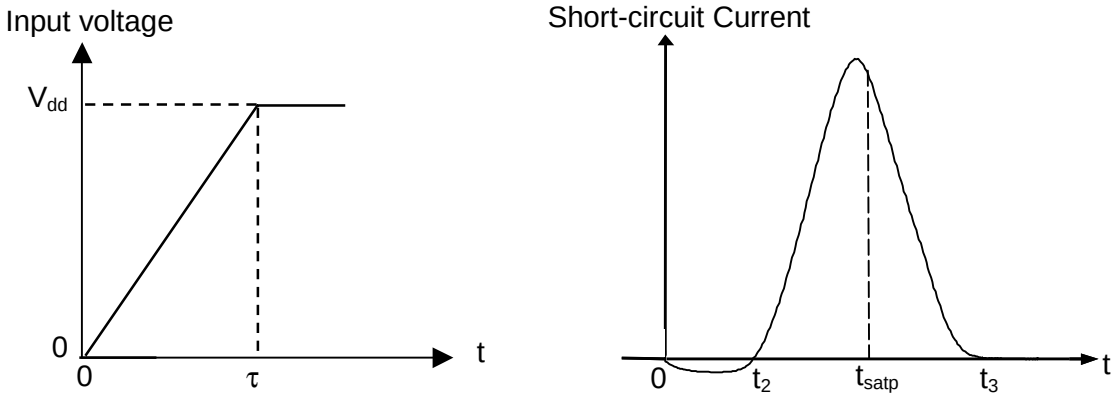

Figure 23. The rising edge of the input pulse and the short-circuit current waveform of a CMOS inverter during this rising edge

the switching energy found through the simulations. Hence, the difference between the energy estimates of the analytical model and the simulations is caused by the short-circuit energy dissipation. The short-circuit energy dissipation of the inverter with parameters in Table 1 is smaller than the short-circuit energy dissipation of the inverter with parameters in Table 2, because the rise and fall times of the input signal are higher in the case of the latter.

In the following section, we first provide a short-circuit energy model for a CMOS inverter. Then we show that our improved analytical model including the short-circuit energy dissipation produces the E-p relationship results that are very close to the results obtained through simulations.

7.2 Modeling the Short-circuit Energy Dissipation of a CMOS Inverter

Our model for the short-circuit energy dissipation is based on the short-circuit energy model presented in [2]. Our model uses the alpha-power (α-power) law MOSFET current model [16]. The model first calculates the short-circuit current. An example waveform for the short-circuit current drawn during the rising edge of a ramp input (V_{in} rising from 0 to V_{dd}) is shown in Figure 23.

In Figure 23, t_2 denotes the point in time when the short-circuit current becomes zero while the PMOS transistor is in linear region. t_{satp} denotes the point in time when the PMOS transistor enters the saturation region, and t_3 denotes the point in time when the short-circuit current becomes zero while PMOS transistor is in saturation region. The details of the derivation of t_2, t_{satp}, and t_3 are presented in [11]. The short-circuit energy consumed during a rising edge of input is described by

$$\begin{aligned} E_{sc}^{r} &= \frac{V_{dd}(t_{satp}-t_2)}{2}\left(\left(S\left(t_{satp}+t_2\right)-2St_1\right)-\frac{2C_{gsp}V_{dd}}{\tau}\right) \\ &-\frac{V_{dd}I_{DOP}}{(V_{dd}-V_{THP})^{\alpha_p}}\left(\left(\frac{V_{dd}t_3}{\tau}-V_{THP}\right)^{\alpha_p+1}-\left(\frac{V_{dd}t_{satp}}{\tau}-V_{THP}\right)^{\alpha_p+1}\right)-\frac{V_{dd}^2C_{gsp}}{\tau}\left(t_3-t_{satp}\right) \end{aligned} \tag{31}$$

where α_p, V_{THP} and I_{DOP} are the empirical parameters of the α-power law MOSFET current model. α_p denotes the velocity saturation index, V_{THP} is the threshold voltage, and I_{DOP} denotes the value of the PMOS transistor saturation current when the gate-to-source voltage of the transistor is equal to V_{dd}. C_{gsp} denotes the gate-to-source capacitance of the PMOS transistor, and τ denotes the input rise time. We estimate the short-circuit current to be linear between t_2 and t_{satp}, and S denotes the slope of the estimated line between t_2 and t_{satp}.

Similarly, the short-circuit energy dissipation of a CMOS inverter during the falling edge of the input is calculated by

$$\begin{aligned} E_{sc}^{f} &= \frac{V_{dd}(t_{satn}-t_2)}{2}\left(\left(S\left(t_{satn}+t_2\right)-2St_1\right)-\frac{2C_{gsn}V_{dd}}{\tau}\right) \\ &-\frac{V_{dd}I_{DON}}{(V_{dd}-V_{THN})^{\alpha_n}}\left(\left(\frac{V_{dd}t_3}{\tau}-V_{THN}\right)^{\alpha_n+1}-\left(\frac{V_{dd}t_{satn}}{\tau}-V_{THN}\right)^{\alpha_n+1}\right)-\frac{V_{dd}^2C_{gsn}}{\tau}\left(t_3-t_{satn}\right) \end{aligned} \tag{32}$$

where the various symbols (such as t_{satn}, C_{gsn}, and V_{THN}) denote the corresponding parameters for the NMOS transistor.

Then, the average short-circuit current consumed by a CMOS inverter per switching is described by

$$E_{sc} = \frac{E_{sc}^{r}+E_{sc}^{f}}{2} \tag{33}$$

The total energy consumed by a CMOS inverter per switching is

$$E = E_{sc} + E_{sw} \tag{34}$$

Using the analytical model in (34) to estimate the energy consumption of the CMOS inverter (with the parameters shown in Table 2) we find the *E-p* relationship shown in Figure 24. As seen in the figure, the analytically obtained *E-p* relationship is very close to the *E-p* relationship obtained through simulations.

7.3 Summary of the Results

In this section, we have improved the analytical model for the energy estimation by including the short-circuit energy dissipation. Short-circuit energy dissipation depends on the supply voltage of the inverter, the load capacitance, the process parameters (especially the threshold voltage and the velocity saturation index), and

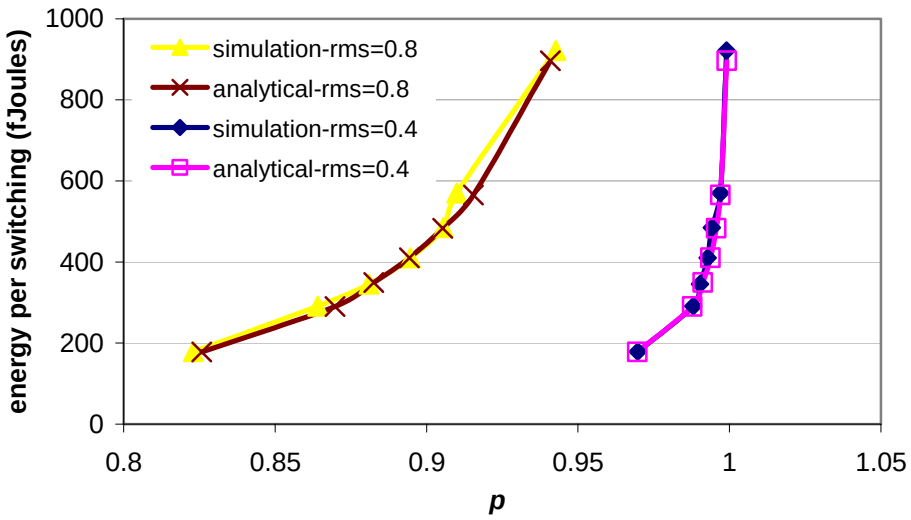

Figure 24. E-p relationship of the CMOS inverter (with the parameters shown in Table 2), wherein the analytical model in (34) is used to estimate the energy consumption of the inverter

the rise and fall times of the input signal. As the feature sizes decrease, the short-circuit energy dissipation might increase due to the decrease in the ratio of V_{th} to V_{dd} [16]. Our model is based on the assumption that the MOSFET drain current is zero in the cutoff region. This assumption does not produce accurate results at small V_{dd} values, because at these values of the supply voltage, the duration of time that the transistors spend in weak inversion region is not negligible. Hence, our model can be improved to include the sub-threshold currents in the weak inversion region.

In the sub-micron regime, another important component of the energy consumption is the leakage energy dissipation. As the technology scales down, not only the sub-threshold current increases due to the scaling of the threshold voltage, but also the gate leakage increases [22]. In order to assure the validity of the E-p relationship in future technologies, we plan to extend our analytical models for the E-p relationship to include the leakage energy dissipation as well.

8. THE IMPACT OF THE OUTPUT SAMPLING FREQUENCY AND THE EQUIVALENT BANDWIDTH OF THE NOISE ON THE PROBABILISTIC BEHAVIOR OF A CMOS INVERTER

In Section 4.1, we defined a probabilistic switch, and in Section 4.2, we described a CMOS inverter equivalent of this probabilistic switch. Our definition of the probabilistic switch imposes some constraints on the sampling frequency of the output, the sampling frequency of the noise, and switching time of the inverter. As we stated in Section 4.2, the switching time of the PCMOS inverter, T_s, is equal to the propagation delay of the inverter. We also assumed that V_{out} is sampled with the same period as the noise is being sampled. To reiterate, we refer to the sampling period of the noise as t_{sn} and the sampling period of V_{out} as t_{so}. By departing from the definition of the probabilistic switch, in Sections 8.1 and 8.2, we will vary the output sampling frequency and the noise sampling frequency, and study the effects of these two parameters on the probabilistic behavior of a CMOS inverter.

In Section 6, we presented the detailed view of the noise pulse (see Figure 11) that is used in circuit simulations and we introduced the two cases of noise sampling. As described in Section 6, in the first case, the noise is latched, and in the second case, the noise is non-latched. Our results in Section 6 were based on the case that

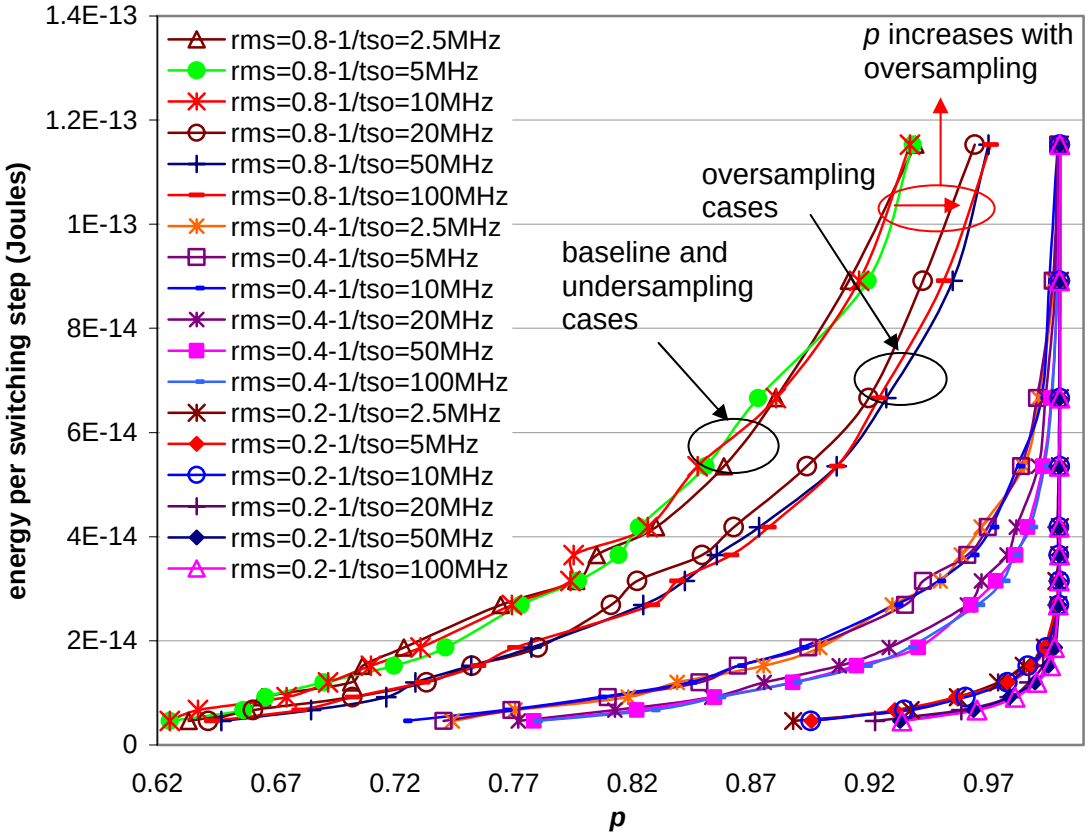

Figure 25. The impact of t_{so} on the E-p relationship when the noise is non-latched

noise is latched. In this section, we will consider only the case that noise is non-latched, because this case constitutes a realistic representation of the noise source [5]. We note that, given that noise is sampled at the rate $\frac{1}{t_{sn}}$, the maximum frequency component of the noise should be smaller than $\frac{1}{2t_{sn}}$ (from Nyquist theorem). We refer to $\frac{1}{2t_{sn}}$ as the equivalent bandwidth of the noise. Hence, in Section 8.2, while varying t_{sn}, we will also be varying the equivalent bandwidth of the noise.

8.1 The Impact of Output Sampling Frequency on the E-p Relationship

To investigate the output sampling frequency effects, we consider (1)*oversampling* wherein the output voltage of the CMOS inverter is sampled more frequently than the output-coupled thermal noise is sampled and (2)*undersampling* wherein the output voltage of the CMOS inverter is sampled less frequently than the output-coupled noise is sampled. As we illustrate later in this section, oversampling has the effect of increasing p (at a fixed value of E) and undersampling does not affect the E-p relationship. We note that, since similar trends are observed in the other cases of noise couplings, we have limited our results to the results obtained in the case of the output-coupled noise.

In this section, in our HSpice simulations, we consider the CMOS inverter with the parameters shown in Table 1 (see Section 6).

Figure 25 shows the impact of the oversampling and undersampling on the E-p relationship in the case of

the output-coupled noise that is non-latched. The sampling frequency ($1/t_{so}$) values of 5MHz and 2.5MHz belong to the case when the output is undersampled. The case when $1/t_{so}$ is equal to 10MHz corresponds to the case that the output is sampled at the same frequency as the noise is sampled, and we refer to this case as the baseline. The sampling frequency values of 100MHz, 40MHz, and 20MHz belong to the case when the output is oversampled.

From the analytical model in (9) (see Section 5.1), p depends on the RMS value (σ) of the noise.In case of oversampling, the effective value of noise RMS is decreased, and thus, the p value is increased (at a fixed value of E). This trend can be seen from Figure 25. Deriving p as a function of (over)sampling frequency is beyond the scope of this paper. However, to show the validity of our simulation results, below, we derive p in case when the sampling frequency is $2/t_{sn}$ and we sketch how to find p for sampling frequency values other than $2/t_{sn}$.

As seen in Figure 25, increasing sampling frequency beyond 20MHz ($2/t_{sn}$) has a negligible impact on the E-p relationship especially at lower noise RMS values as shown in Table 3, which shows the average value of p at RMS values of 0.4V and 0.8V at different values of output sampling frequency. For example, Table 3 shows that, when RMS value of the noise is 0.4V, the difference between p values for the cases of $1/t_{so}$=20MHz and $1/t_{so}$=40MHz is only 0.646%, and for the cases of $1/t_{so}$ = 20MHz and t_{so} = 100MHz it is 0.753% on the average.

In the case of undersampling, however, the effective RMS value of noise remains the same (provided that the number of output samples is large enough to preserve the original Gaussian distribution), and hence p is not affected. Therefore, we expect undersampling not to have an impact on the E-p relationship, which is validated through the simulation results shown in Figure 25.

	Noise RMS = 0.4V			Noise RMS = 0.8V		
	Output sampling frequency ($1/t_{so}$)			Output sampling frequency ($1/t_{so}$)		
	20MHz	40MHz	100MHz	20MHz	40MHz	100MHz
Average value of p	0.929	0.935	0.936	0.807	0.818	0.817

Table 3. The variation in the average value of p across different noise RMS values and output sampling frequencies

8.1.1 *Oversampling at a Frequency of* $2/t_{sn}$. As we stated before, in the case that the noise is non-latched, t_{nc} (see Figure 11) is identical to 0. To reiterate, in the case of noise being non-latched, the noise voltage source used in HSpice simulations isa piecewise linear voltage source, which is often used to realize transient simulations with noise [5]. Hence, in the case of output-coupled noise, the output voltage is also a piecewise linear signal. Figure 26 shows the output voltage waveform and the corresponding samples in the cases that output voltage is sampled at the rate $1/t_{sn}$ (baseline) and at the rate $2/t_{sn}$ (oversampling).

In Figure 26, the samples denoted by y_i represent the output samples obtained at the rate $1/t_{sn}$, while the samples denoted by z_i represent the additional output samples obtained at the rate $2/t_{sn}$. Note that at the sampling rate $2/t_{sn}$, the set of output samples is $z_1, z_2, \cdots, z_N, y_1, y_2, \cdots, y_N$ as shown in the figure. We denote the set of y_is by Y and the set of z_is by Z. Hence, $Y = \{y_1, y_2, y_3, \cdots, y_{n-1}, y_n\}$ and $Z = \{z_1, z_2, z_3, \cdots, z_{n-1}, z_n\}$. $C(Y)$ denotes the cardinality of Y and $C(Z)$ denotes the cardinality of Z.

To reiterate, p (obtained through simulations) is equal to the ratio of the number of the correct simulation points to the ratio of the total number of simulation points. Hence, the probability of being correct for the case that the output being sampled at the rate $1/t_{sn}$, denoted p_{sn}, can be described as follows

$$p_{sn} = \frac{\text{\# of correct simulation points (at sampling rate } 1/t_{sn})}{\text{total \# of simulation points (at sampling rate } 1/t_{sn})} = \frac{C\left(Y_c\right)}{C\left(Y\right)} \tag{35}$$

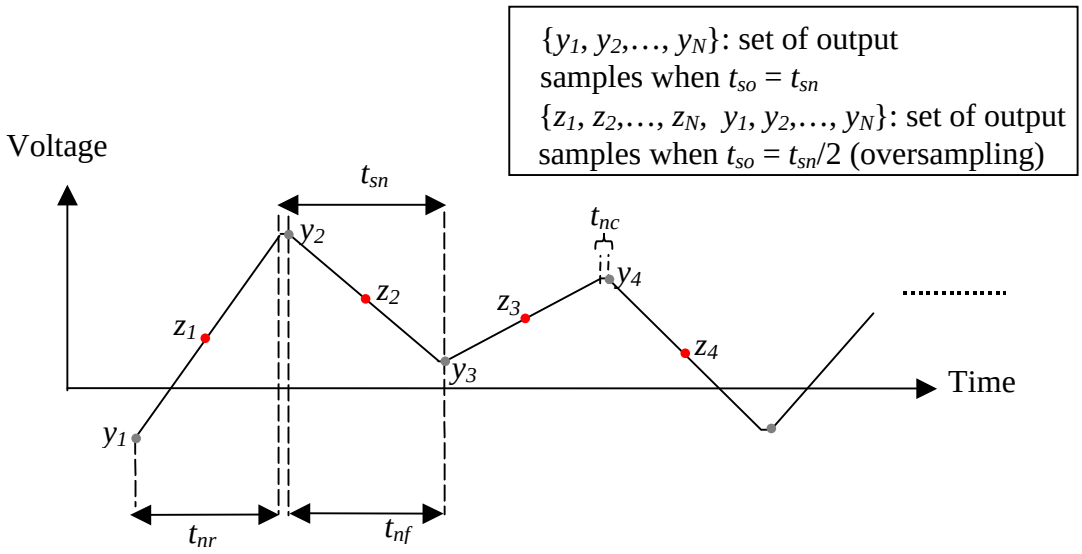

Figure 26. The output voltage waveform and the output samples with/without oversampling

where Y_c denotes the set of the correct simulation points in Y. Similarly, Z_c denotes the number of correct simulation points in Z.

Then, in the case of output being oversampled, the probability of being correct is denoted by p_{OS} and is described as follows

$$p_{OS} = \frac{\#\text{ of correct simulation points (at sampling rate } 2/t_{sn})}{\text{total }\#\text{ of simulation points (at sampling rate } 2/t_{sn})} = \frac{C(Y_c) + C(Z_c)}{C(Y) + C(Z)} \tag{36}$$

Since, the oversampling is realized at the rate $2/t_{sn}$, $C(Y) = C(Z) = N$, where N denotes the total number of simulation points in the case that the output is sampled at the rate t_{sn}. Thus,

$$p_{OS} = \frac{C(Y_c) + C(Z_c)}{2N} = \frac{1}{2}\frac{C(Y_c)}{N} + \frac{1}{2}\frac{C(Z_c)}{N} \tag{37}$$

Now, let us consider the two sets, Y and Z both of which have a cardinality of N. The probability of being correct for set Y, denoted by p_Y, is expressed by the ratio $\frac{C(Y_c)}{N}$. Similarly, the probability of being correct for set Z, denoted by p_Z is expressed by the ratio $\frac{C(Z_c)}{N}$. Hence, in case of output being oversampled at the rate $2/t_{sn}$, from (37)

$$p_{OS} = \frac{p_Y + p_Z}{2} \tag{38}$$

Below, using the analytical model of p, which was described in Section 5.1, we show that p_Y and p_Z can be expressed as a function of the RMS value of the noise and the supply voltage, and we derive a relationship between p_{OS} and p_{sn}.

Referring to Figure 26, when the output is sampled at the rate $2/t_{sn}$, an element (output sample) z_i in Z, is related to two consecutive elements, y_i and y_{i+1}, of Y as follows

$$z_i = \frac{y_i + y_{i+1}}{2} \tag{39}$$

Below, we first show that the elements of Y and Z come from a Gaussian distribution. Second, we calculate the RMS value of the Gaussian distribution that the elements in Z are derived from.

LEMMA 8.1. *In the case of the output being sampled at the rate $1/t_{sn}$, each element in Y comes from a Gaussian distribution with* RMS *value of σ, wherein σ is also the* RMS *value of the Gaussian distribution of the thermal noise coupled to the output of the inverter.*

PROOF. Since the noise under consideration is output-coupled thermal noise, $V_{out}(t) = V_o(t) + {V_n}^*(t)$ where $V_o(t)$ denotes the voltage difference of the drain nodes of the inverter transistors from the ground as shown in Figure 3 (see Section 4.2) at a point in time, t. Since the output voltage is sampled at the same rate as the noise is sampled ($1/t_{sn}$), if the output is sampled at time t', $V_{out}(t')$ corresponds to the sum of ${V_n}^*(t')$ and $V_o(t')$, and this is valid for every such t' (every such sample). Furthermore, the input of the inverter is kept constant, hence $V_o(t)$ is also constant. The proof follows from the fact that for a random variable $\mathbf{x}$ having a Gaussian distribution with variance σ^2, $\mathbf{x}$+C (C is constant) also has a Gaussian distribution with variance σ^2 [21]. □

In the following lemma and proof, we consider only the case that C is zero. If C is not zero, we can define another set Z^*, such that each element of Z^*, of which is identical to z_i-C (i is an integer in [1, N]). The following lemma and proof is also valid for Z^*.

LEMMA 8.2. *In the case of the output being sampled at the rate $2/t_{sn}$, each element in Y comes from a Gaussian distribution with* RMS *value of σ and each element in Z comes from a Gaussian distribution with* RMS *value of σ_Z, wherein σ_Z is approximately equal to $\frac{\sigma}{\sqrt{2}}$.*

PROOF. Each element in Y comes from a Gaussian distribution with RMS value of σ follows from Lemma 8.1.

From (39), each element in Z is a linear combination of the elements in Y. Hence each element in Z also comes from a Gaussian distribution [21]. Using (39) and the definition of the variance, the variance of the Gaussian distribution for the elements in Z, σ_Z, is described by

$$\sigma_Z = \frac{1}{N}\sqrt{\frac{y_1^2+y_2^2+y_3^2\ldots+y_n^2}{4} + \frac{y_2^2+y_3^2+y_4^2\ldots+y_{n-1}^2}{4} + \frac{2y_1y_2+2y_2y_3+\ldots+2y_{n-1}y_n}{4}} \tag{40}$$

In (40), the third ratio in the square root is equal to 0, since the elements in Y are uncorrelated. From here, Lemma 8.2 follows.

□

Then, from (9) (see Section 5), (38), and Lemma 8.2, we can calculate p_Y and p_Z, and show that

$$p_{OS} = \frac{1}{2} + \frac{1}{8}erf\left(\frac{V_m}{\sqrt{2}\sigma}\right) + \frac{1}{8}erf\left(\frac{V_{dd}-V_m}{\sqrt{2}\sigma}\right) + \frac{1}{8}erf\left(\frac{V_m}{\sigma}\right) + \frac{1}{8}erf\left(\frac{V_{dd}-V_m}{\sigma}\right) \tag{41}$$

Since $p_Z > p_Y$,

$$p_{OS} = \frac{p_Y + p_Z}{2} > p_Y = p_{sn} \tag{42}$$

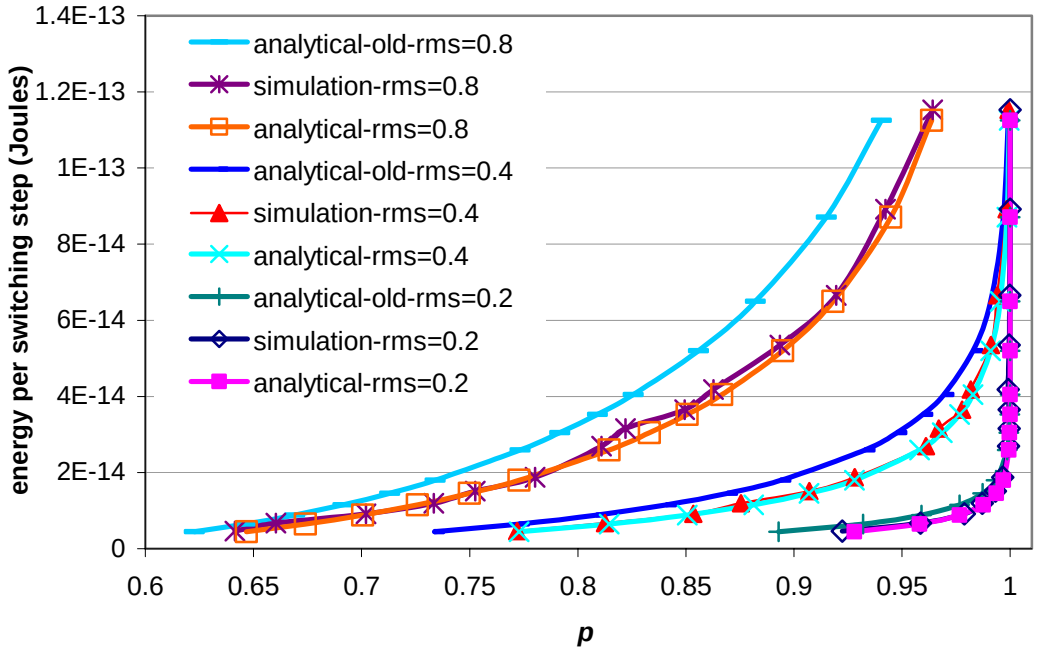

Figure 27. The E-p relationship in the case of the output being sampled at $2/t_{sn}$ and the noise is non-latched

Figure 27 shows a comparison of the analytically calculated E-p relationship (using (41)) and the E-p relationship obtained through the simulations when the output is sampled at the rate $2/t_{sn}$. In this figure, we also show the analytical E-p relationship obtained using (9). As seen in the figure, the results obtained using the analytical model of (41) show strong matched with the simulation results unlike the results of the analytical model using (9) (which we refer to as the analytical-old in the figure).

8.1.2 *A Sketch of Analytical Model of p when the Output Voltage is Oversampled.* In the case of the output being sampling at the rate $2/t_{sn}$, we identified the sets Y and Z. Similarly, in the case of other sampling rates, $1/t_{so} > 1/t_{sn}$, we can identify such sets, and find the probability of being correct for each set. We can also express p_{OS} in terms of the values of probability of being correct for these sets and show that p_{OS} is always larger than the probability of being correct in the case of the baseline.

As we previously showed in Figure 25, oversampling beyond $2/t_{sn}$, that is, $1/t_{so} > 2/t_{sn}$, has a negligible impact on p, especially at lower values of the RMS value of the noise. Referring to Figure 25, at an RMS value of 0.8V and at a fixed value of E, p increases when sampling frequency increases from 20MHz to 50MHz for p >0.8. However, we do not observe a steady increase in p as the frequency of sampling increases. This is because of the averaging of the probability values similar to the case of averaging for the sampling rate $2/t_{sn}$ as described by (38). Furthermore, it can be shown that p_{OS} will always be lower than p_Z (probability of being correct in the instance of sampling at the rate $2/t_{sn}$).

8.2 The Impact of the Equivalent Noise Bandwidth on the E-p Relationship

In this section, we investigate the impact of the equivalent bandwidth of the noise on the E-p relationship of an inverter with input-coupled thermal noise. In our circuit simulations, we consider the case that noise is non-latched. Given that noise is sampled at the rate $\frac{1}{t_{sn}}$, the maximum frequency component of the noise

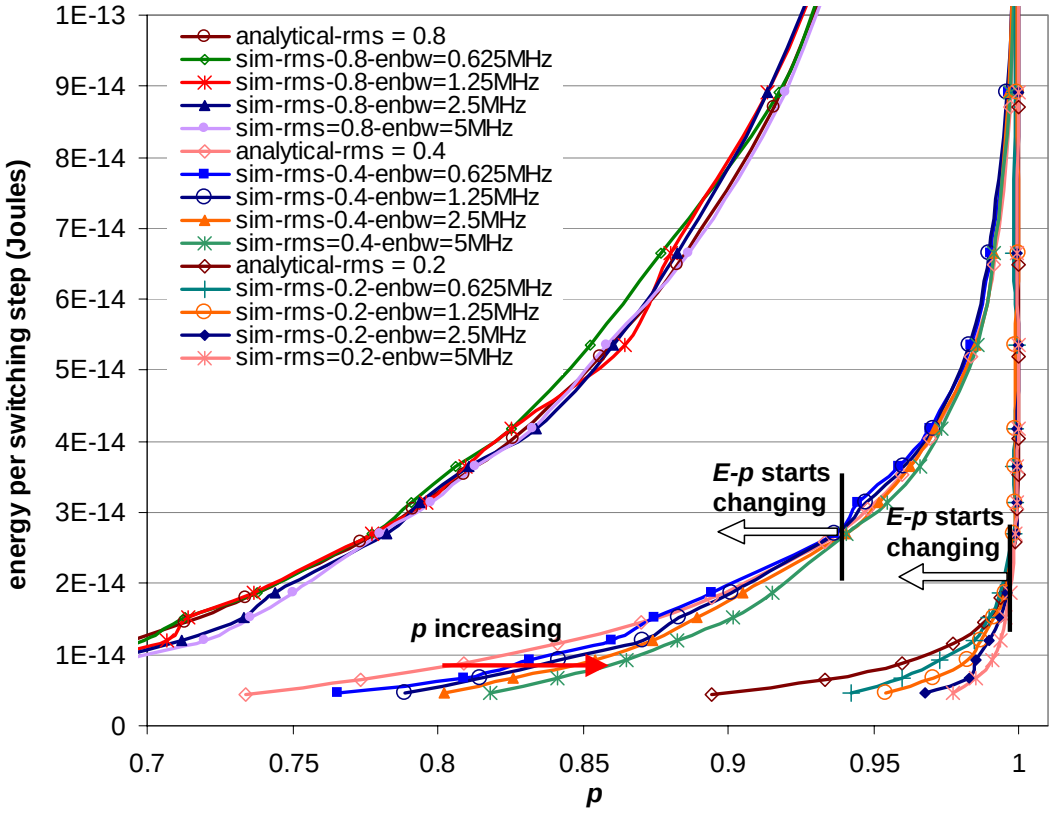

Figure 28. The E-p relationship for different values of ENBW

should be smaller than $\frac{1}{2t_{sn}}$ (from Nyquist theorem). We refer to $\frac{1}{2t_{sn}}$ as the equivalent bandwidth of the noise, denoted ENBW. Note that in the results shown below, the noise and the output are sampled at the same frequency ($\frac{1}{t_{sn}} = \frac{1}{7}t_{so}$).

In Figure 28, we show the E-p relationship of the CMOS inverter with the parameters shown in Table 1 (see Section 6) for different values of equivalent noise bandwidth ENBW and for different values of noise RMS. The E-p relationship curves for different values of ENBW are obtained through HSpice simulations. The analytical E-p relationships, on the other hand, are obtained using (9). As seen in the figure, ENBW has a negligible impact on the E-p relationship for the noise RMS value of 0.8V. However, for the noise RMS values of 0.4V and 0.2V, we observe that E-p relationship starts changing with ENBW after a specific value of p is reached as shown in the figure. For example, when the RMS value of noise is 0.4V, we observe that p starts increasing at a fixed value of E as ENBW increases when $p < 0.94$. This change in the E-p relationship is caused by the change in p due to the change in ENBW. Figure 29 shows p with respect to V_{dd} at different values of noise RMS value and ENBW.

As seen in Figure 29, especially for small RMS values of the noise (0.4V and 0.2V) p starts changing with ENBW after a specific value of p (that is, after a specific value of V_{dd}) is reached, similar to the E-p relationship shown in Figure 28. In particular, at small RMS values of the noise, at a fixed value of V_{dd}, p increases as ENBW increases if V_{dd} is smaller than a specific value. As V_{dd} decreases, the propagation delay of the inverter increases, and the duration of the noise pulse (t_{sn}) at the input becomes relatively shorter (than the propagation

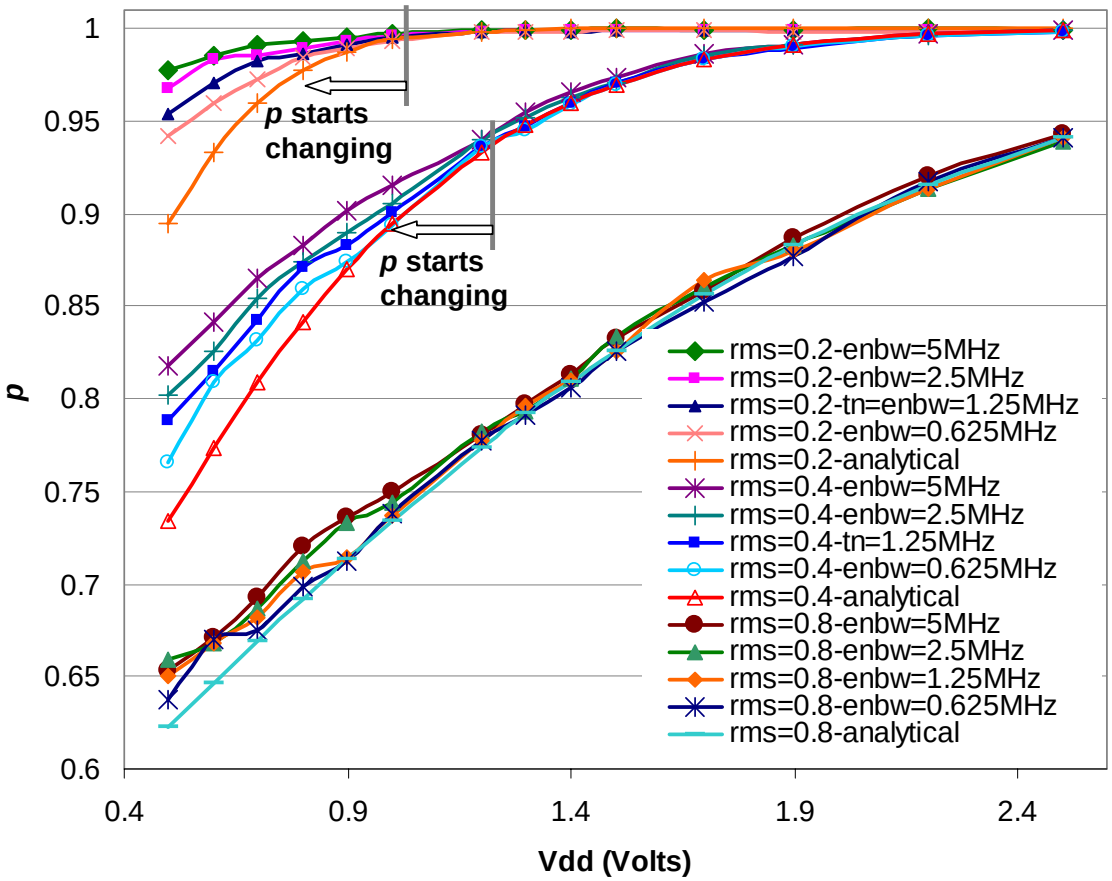

Figure 29. The change in p with respect to V_{dd} for different values of noise RMS and different values of t_{sn}

delay of the inverter) for the errors (caused by the noise at the input) to be propagated to the output of the inverter. This trend in p is more prominent at small noise RMS values, since the input-coupled noise with a small RMS value also translates to a small input voltage, which increases the propagation delay of the inverter even further. We note that propagation delay of the inverter is dependent on the input voltage. For example, for the CMOS inverter with the characteristics summarized in Table 1 and with a supply voltage of 0.6V, the propagation delay in the case of an input pulse changing from 0V to 0.6V is ∼4ns, whereas it is ∼13ns in the case of an input pulse changing from 0.1V to 0.6V.

8.3 Summary of the Results

In this section, we have investigated the impacts of the output sampling frequency and the equivalent bandwidth of the noise on the E-p relationship. Since the case of the noise being non-latched constitutes a more realistic way of modeling noise and the piecewise linear voltage source based noise source is the commonly used noise source in transient circuit simulations [5]; in the above section, we have considered only the instance of noise being non-latched.

In the context of the output sampling, we have seen that oversampling, in which case the output is sampled at a higher rate than the noise is being sampled, increases p (at a fixed value of E). Hence, if our probabilistic

inverter is utilized as a random bit generator, wherein the output of the inverter is sampled using another circuitry, and the noise is non-latched, the output sampling frequency should be chosen to be less than the noise sampling frequency. We have derived an analytical model for the case of oversampling at $2/t_{sn}$ and sketched a way of deriving analytical expressions in the case of oversampling at rates other than $2/t_{sn}$.

In this report, in the context of the impact of the output sampling on the E-p relationship, we have limited ourselves with the results for the case of output-coupled noise. We note that similar trends are observed in other cases of noise couplings.

In studying the impact of the equivalent bandwidth of the noise on the E-p relationship, we have only considered the case of the input-coupled noise, wherein the switching time is identical to the propagation delay of the inverter (see the definition of the probabilistic switch in Section 4.1). We have observed that, at a fixed value of E, as the equivalent bandwidth of the noise increases, p increases. In the case of the power supply noise, we have observed similar trends in the E-p relationship. However, the impact of these two parameters is less prominent in the case of the output-coupled noise.

Our study of the impact of equivalent bandwidth of the noise is limited to HSpice simulations. Estimating the output of an inverter that is coupled with noise at its input involves an analysis of the nonlinear large signal behavior of the inverter, and is beyond the scope of this paper.

9. REMARKS ON THE IMPACT OF SPURIOUS SWITCHINGS DUE TO NOISE ON THE ENERGY CONSUMPTION OF A CMOS INVERTER

In the previous sections, we have considered the energy consumed by a CMOS inverter per switching, wherein the switching is considered to be a change of the output of the inverter from a 0 to V_{dd} or vice versa. However, in the case that noise is coupled to an inverter, the inverter output undergoes many spurious variations due to noise and it consumes additional energy due to these spurious invocations. Hence, given a probabilistic CMOS inverter and a deterministic CMOS inverter, wherein the deterministic inverter produces a correct output with a probability nearly equal to 1 (with probability of error as small as 10^{-19}) and the probabilistic inverter produces a correct result at the output with a probability p ($0.5 < p < 1$), the probabilistic inverter might consume more energy than its deterministic counterpart in a time interval, T, during which the deterministic inverter undergoes switchings due to changes at its input voltage while probabilistic inverter undergoes switchings due to the changes at its input as well as the spurious switchings due to the noise.

		Deterministic inverter	**Probabilistic inverter**
Inverter fan-out		4	4
Load capacitance		28fF	28fF
Nominal Vdd (V)		2.5	2.5
Inverter transistor sizes	$\mathbf{(W/L)}_{pmos}$	2u/0.3u	2u/0.3u
	$\mathbf{(W/L)}_{nmos}$	0.8u/0.3u	0.8u/0.3u
Vdd (V)		1.5-2.5	0.5-2.5
σ **(V)**		0	0.2-0.8
Input rise and fall time		0.2ns	0.2ns

Table 4. Simulation parameters for the deterministic and probabilistic inverters

We note that we now consider the energy consumed by a CMOS inverter during a time interval T, instead of during the switching time, T_s. In Figure 30, we demonstrate the effect of these spurious switchings on the energy consumption of a probabilistic inverter. This figure shows the HSpice simulation results for the energy consumed in 100μs by a deterministic inverter and a probabilistic inverter implemented in TSMC 0.25μm. The simulation parameters for the inverters are shown in Table 9. Figure 30 demonstrates that the probabilistic

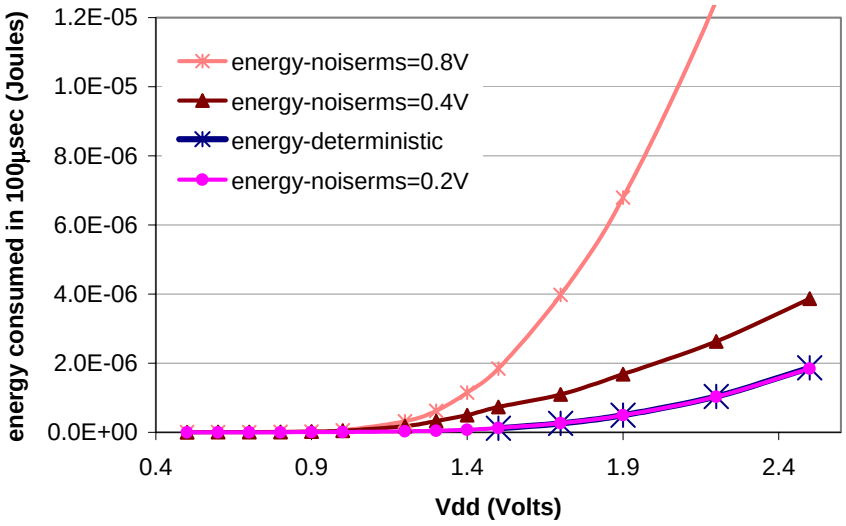

Figure 30. The energy consumed in 100μs by a deterministic inverter and probabilistic inverter

inverter consumes more energy than the deterministic inverter in the case that the noise RMS value is larger than 0.2V. For example, in the case that RMS value of the noise is 0.4V and the supply voltage is 1.7V, the probabilistic inverter consumes 2.126μJ, whereas the deterministic inverter with the same supply voltage consumes 1.165μJ. In the case that noise RMS value is 0.2V, the probabilistic inverter consumes less power than the deterministic inverter.

10. CONCLUDING REMARKS

In this report, we have presented an extensive study of the E-p relationship of a CMOS inverter. We have considered different couplings of noise, which include the input-coupling of thermal noise, output-coupling of thermal noise and/or power supply noise coupling. The analytical models we have developed for different cases of noise couplings strongly match with the simulation results strongly. We have also studied the impact of the output sampling frequency, noise duration and the equivalent bandwidth of the noise on the E-p relationship.

We have demonstrated that the type of coupling of the noise has a significant impact on the probabilistic behavior of a CMOS inverter. In a scenario where many noise sources are coupled to a CMOS inverter, it is quite important and difficult to model the aggregated impact of these noise sources successfully.

In our work, we have only considered controllable noise sources, that is, the distribution and the frequency spectrum of noise sources are known a priori. Given the controllable noise sources, we have demonstrated that noise can be utilized to realize probabilistic computation with a specific probability p.

Furthermore, the circuitry that is sampling the output of a probabilistic inverter has to be designed carefully, and the sampling frequency should be known by the designer so that the probabilistic behavior of the inverter can be estimated a priori.

Our work provides analytical models and insights to the circuit designers who might want to utilize noise to realize probabilistic circuits. In addition, using our analytical models, one can design circuits and architectures based on these circuits as demonstrated in [19].

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