

# Lakshmi N. B. Chakrapani

## *Curriculum Vitae*

### Contact

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### Areas of Interest

Probabilistic Design, Probabilistic Architectures, Adaptive Architectures, Compilation for High Performance, Embedded and Adaptive Architectures, High-level Synthesis of Application-specific Architectures, and Machine Learning for Platform-aware Compilation

### Education

08/2008

#### **Ph.D. in Computer Science**

College of Computing, Georgia Institute of Technology, Atlanta, GA

Thesis: *Probabilistic Boolean Logic, Arithmetic, and Architectures*

Minor in Electrical Engineering (Physical CAD and Synthesis)

05/2000

#### **B.E. in Computer Science and Engineering**

College of Engineering, Guindy, Anna University, Chennai, India

Thesis: *An FPGA-based Indian Arithmetic Co-processor*

### Honors and Recognition

2008

#### **Georgia Institute of Technology Sigma Xi Best Thesis Award**

Awarded in 2009 to five dissertations from about five hundred dissertations university-wide and was also nominated by the College of Computing at Georgia Institute of Technology for the ACM doctoral dissertation award

2008

#### **“10 technologies that we think are most likely to change the way we live”**

Technology Review (Published by MIT) in its special report on 10 Emerging Technologies of 2008 ranked “*Probabilistic Chips*” based in part on my dissertation, as one of the “*10 technologies that we think are most likely to change the way we live*”

### Technical Skills

Design and implementation of algorithms for program analysis and optimization, design and analysis of randomized algorithms, compiler development, software development with C and C++ in Unix/Linux environment, scripting languages, various architecture simulators

### Specific Technical Skills and Research Experience

#### **Probabilistic Design**

- Areas: Research, development and application of techniques in *mathematical logic, randomized algorithms, analysis of algorithms, algorithmic complexity, tail bound analysis of sum of random variables, and probabilistic computing architectures.*
- Infrastructure: C, C++, scripting in Linux environment, and development and use of in-house simulation tool

### **Compilation and High-level Synthesis of Custom and Adaptive Architectures**

- Areas: Research, development and application of techniques in *Compiler optimizations targeting the use of the memory hierarchy, compiler optimizations for energy efficient computing, performance analysis of programs, program analysis and optimization for high-level synthesis of application-specific architectures*
- Infrastructure: The Trimaran system, C, C++, scripting in Linux environment and use of linear programming libraries

### **Machine Learning for Platform-aware Compilation**

- Areas: Research, development and application of techniques in *Machine learning, program analysis and optimization, and performance analysis of applications*
- Infrastructure: PACE compiler infrastructure, in-house infrastructure for machine learning through neural networks and self-organizing maps

## **Employment**

- 06/2010–Present **Research Scientist**  
Department of Computer Science, Rice University, Houston, TX
- 09/2008–06/2010 **Postdoctoral Research Associate and External Relations Coordinator of VISEN Center**  
Department of Computer Science, Rice University, Houston, TX
- 10/2007–09/2008 **Staff** (Visiting Graduate Student) – Research on Probabilistic Design  
Department of Computer Science, Rice University, Houston, TX
- 03/2007–09/2007 **Visiting Graduate Student** (Supported by Georgia Institute of Technology)  
Computer Science Department, California Institute of Technology, Pasadena, CA
- 08/2000–03/2007 **Graduate Research Assistant**  
Also Graduate Teaching Assistant for CS 3240 Languages and Computation  
and Graduate Teaching Assistant for CS 6241 Compiler Design in 2006  
Center For Research on Embedded Systems and Technology  
Georgia Institute of Technology, Atlanta, GA
- 05/2004-08/2004 **Research Intern**  
Hewlett Packard Laboratories  
Palo Alto, CA

## **Research Funding**

- 04/2009–03/2011 **Probabilistic Design of Computing Systems Based on Novel Materials and Value of Information** (Co-Principal Investigator)  
Nanyang Technological University, Singapore, funded \$664,294

## **Patents**

- 2010 **Computing Device Using Inexact Computing Architecture Processor**  
Krishna V. Palem, Lakshmi N. B. Chakrapani and Avinash Lingamneni, Patent Cooperation Treaty (PCT) Patent Application No. PCT/US2010/026686, 2010

## **Selected Press Coverage**

- 03/2009 “Probably the best logic in the world,” by Eric Doyle, *Computer Weekly*, March 22, 2009
- 02/2009 “A Chip That Is Probably Right,” by Jonathan Fahey, *Forbes Online*, February 26, 2009

03/2005            “Toward More Efficient Computers: Researchers Validate Energy Savings of P-Bits,” *Science Daily*, March 5, 2005

## Professional References

Available upon request

## Professional Service

### Member of the Technical Program Committee

- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Part of Embedded Systems Week (ESWeek), Scottsdale, AZ, October 2010
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Part of Embedded Systems Week (ESWeek), Grenoble, France, October 2009

### Member of the Organizing Committee

- Symposium on Transformational Information Engineering and Science, Nanyang Technological University, Singapore, January 28-29, 2010
- Workshop on Sustainable Nanoelectronics and Information Technology, Rice University, Houston, TX, June 24, 2009

### Reviewer

- Communications of the ACM, The Computer Journal, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), and other Conferences and Journals

## Publications

### Probabilistic Design

**Lakshmi N. B. Chakrapani** and Krishna V. Palem. A probabilistic Boolean logic for energy efficient circuit and system design. In *Proceedings of the 2010 Asia and South Pacific Design Automation Conference (ASPDAC)*, 2010.

Krishna V. Palem, **Lakshmi N. B. Chakrapani**, Zvi M. Kedem, Avinash Lingamneni, and Kirthi Krishna Muntimadugu. Sustaining Moore’s law in embedded computing through probabilistic and approximate design: Retrospects and prospects. In *Proceedings of the 2009 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 1–10, 2009.

**Lakshmi N. B. Chakrapani**, Jason George, Bo Marr, Bilge E. Akgul, and Krishna V. Palem. Probabilistic design: A survey of probabilistic CMOS technology and future directions for terascale IC design. In *VLSI-SoC: Research Trends in VLSI and Systems on Chip*, volume 249, pages 101–118. 2008.

**Lakshmi N. B. Chakrapani**, Kirthi Krishna Muntimadugu, Avinash Lingamneni, Jason George, and Krishna V. Palem. Highly energy and performance efficient embedded computing through approximately correct arithmetic: A mathematical foundation and preliminary experimental validation. In *Proceedings of the 2008 International Conference on Compilers, Architecture, and Synthesis of Embedded Systems (CASES)*, 2008.

**Lakshmi N. B. Chakrapani**, Pinar Korkmaz, Bilge E. Akgul, and Krishna V. Palem. Probabilistic system-on-a-chip architectures. *ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES)*, 12(3):1–28, August 2007.

**Lakshmi N. B. Chakrapani**, Bilge E. S. Akgul, Suresh Cheemalavagu, Pinar Korkmaz, Krishna V. Palem, and Balasubramanian Seshasayee. Ultra efficient embedded SOC architectures based on probabilistic CMOS technology. In *Proceedings of The 9th Design Automation and Test in Europe (DATE)*, pages 1110–1115, March 2006.

Babak Firoozbakhsh, Nikil Jayant, and **Lakshmi N. B. Chakrapani**. MAC layer mitigation of interference between IEEE 802.11a and ultra wideband (UWB) systems. In *Proceedings of the International Conference on Communications in Computing*, 2006.

Pinar Korkmaz, Bilge E. S. Akgul, **Lakshmi N. B. Chakrapani**, and Krishna V. Palem. Advocating noise as an agent for ultra low-energy computing: Probabilistic CMOS devices and their characteristics. *Japanese Journal of Applied Physics (JJAP)*, 45(4B):3307–3316, April 2006.

Bilge E. Akgul, **Lakshmi N. B. Chakrapani**, Pinar Korkmaz, and Krishna V. Palem. Probabilistic CMOS technology: A survey and future directions. In *Proceedings of the IFIP International Conference on Very Large Scale Integration*, pages 1–6, October 2006.

Suresh Cheemalavagu, Pinar Korkmaz, Krishna V. Palem, Bilge E. Akgul, and **Lakshmi N. B. Chakrapani**. A probabilistic CMOS switch and its realization by exploiting noise. In *Proceedings of the IFIP international conference on very large scale integration*, 2005.

### Compilers, Embedded Systems and Customization

**Lakshmi N. B. Chakrapani**, John Gyllenhaal, Wen mei W. Hwu, Scott A. Mahlke, Krishna V. Palem, and Rodric M. Rabbah. Trimaran: An infrastructure for research in instruction-level parallelism. In *Proceedings of The 17th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, volume 3602, pages 32–41. Springer-Verlag Berlin Heidelberg, August 2005.

Krishna V. Palem, **Lakshmi N. B. Chakrapani**, and Sudhakar Yalamanchili. A framework for compiler driven design space exploration for embedded system customization. In *Proceedings of the 9th Asian Computing Science Conference*, 2004.

Kiran Puttaswamy, **Lakshmi N. B. Chakrapani**, Kyu-Won Choi, Yuvraj Singh Dhillon, Utku Diril, Pinar Korkmaz, Kyoung-Keun Lee, Jun Cheol Park, Abhijit Chatterjee, Peeter Ellervee, III Vincent John Mooney, Krishna V. Palem, and Weng-Fai Wong. Power-performance trade-offs in second level memory used by an ARM-like RISC architecture. In Robert Graybill and Rami Melhem, editors, *Power aware computing*, pages 211–224. Kluwer Academic Publishers, Norwell, MA, USA, 2002.

**Lakshmi N. B. Chakrapani**, Pinar Korkmaz, Vincent John Mooney, Krishna V. Palem, Kiran Puttaswamy, and Weng-Fai Wong. The emerging power crisis in embedded processors: What can a compiler do? In *Proceedings of the IEEE/ACM International Conference on Compilers, Architecture and Synthesis for Embedded Systems*, pages 176–180, 2001.

Ranjani Parthasarathi, Easwaran Raman, Karthik Sankaranarayanan, and **Lakshmi N. B. Chakrapani**. A reconfigurable co-processor for variable long precision arithmetic. In *The 9th Annual IEEE Symposium on Field-Programmable Custom Computing Machines*, pages 71–80, 2001.

### Manuscripts Under Preparation and Review

**Lakshmi N. B. Chakrapani** and Krishna V. Palem. A probabilistic Boolean logic and its meaning. *Rice University, Department of Computer Science Technical Report*, (TR-08-05), June 2008.

**Lakshmi N. B. Chakrapani** and Krishna V. Palem. Working title: New results in large deviations and their application to probabilistic arithmetic. *Under Review*, 2010.

### Selected Talks

*What to Do About the End of Moore's Law (Probably)?* Department of Statistics Colloquium, Rice University, January 2009

*Highly Productive Compiler-Driven Customization of Heterogeneous Embedded Platforms*, Workshop on Compiler Assisted SoC Assembly (CASA), Embedded Systems Week, Seoul, Korea, October 2006

*Probabilistic CMOS Technology for Embedded Cognitive Information processing*, High Performance Embedded Computing Workshop, MIT Lincoln Laboratory, Lexington, MA, September 2006

*Probabilistic Architectures*, Intel Corporation, Portland, OR, July 2006

*Trimaran: An Infrastructure for Research in Instruction-Level Parallelism*, Languages and Compilers for Parallel Computing (LCPC) Workshop on Compiler Research Infrastructures, West Lafayette, IN, September 2004

## Description of Research Experience

### **Probabilistic Design (2003-Present)**

Increasing power density and device perturbations due to noise are some of the severe impediments to sustained scaling down of transistor feature sizes (Moore's law). My dissertation work studied the theoretical and practical aspects of energy efficient and high performance computing in the presence of these perturbations. Specifically, my dissertation defined a new mathematical logic, the *Probabilistic Boolean Logic* (PBL) which reasons about Boolean algebra and Probability in an unified framework. PBL enables logic synthesis with unreliable building blocks (such as gates), for low energy and high performance implementations of probabilistic applications using and novel class of *Probabilistic Architectures*. The energy and performance advantages of Probabilistic Architectures were demonstrated in my dissertation through simulations using circuit simulation tools and through subsequent fabrication and measurement of one of the designs by my colleagues. Based on PBL, I defined *Probabilistic Arithmetic* (PA) operations which are arithmetic operations susceptible to errors. The utility of PA was demonstrated through VLSI implementations of digital signal processing applications where the quality of the signal, such as those of audio and video, may be traded for gains in energy and processing time of the circuit. This work was supported in part by DARPA under seedling contract #F30602-02-2-0124, an award from Intel Corporation, By the Nanyang Technological University in Singapore and by the VISEN center at Rice University.

### **Compilation for High Performance and Embedded Systems (2000-2005)**

As part of the Trimaran ( <http://www.trimaran.org/> ) compiler development team, I conducted research and implemented algorithms for analysis and optimization of programs for the efficient use of energy and the memory hierarchy. Trimaran is an infrastructure with an open source compiler, an architecture description language and parametric simulator, collaboratively developed by the Hewlett Packard Corporation, University of Illinois at Urbana-Champaign and Georgia Institute of Technology. Trimaran targets high performance, embedded and adaptive EPIC architectures and has been used for teaching and research in over 40 universities resulting in over 150 peer-reviewed publications. This work was supported in part by an award from the Hewlett Packard Corporation and the DARPA Power-Aware Computation and Communication program.

### **Compilation for Adaptive Architectures and Customization (2003-2005)**

The productivity of designers of application specific custom architectures can be tremendously improved by high-level synthesis—the synthesis of application-specific architectures from programs written in high level languages. I was part of a team that developed the Trimaran-based TRIX compiler, which synthesizes the architectural description of application-specific processors based on applications written in a subset of the C language. This architecture can in turn be implemented on a programmable polymorphic substrate (specifically, the MONARCH architecture developed by Raytheon Corporation). Alternately, by combining a database of pre-synthesized architectural components and by using algorithms that perform component selection as well as placement and routing, an architectural design of a non-programmable customized Application Specific Integrated Architecture (ASIC) could be produced by TRIX. This work was supported in part by DARPA Polymorphic Computing Architectures Program under contract #F33615-03-C-4105.

### **Machine Learning for Platform-aware Compilation (2009-Present)**

This work is supported by DARPA through AFRL Contract #FA8650-09-C-7915 as a part of the “Platform Aware Compilation Environment” (PACE) project ( <http://www.rice.edu/nationalmedia/news2009-04-07-darpa.shtml> ). The aim of this project is to reduce the time required to produce high-quality compilers for new computer systems. As part of this project, I am conducting research on the use of Machine Learning techniques to effectively and efficiently characterize the interactions between programs, target systems, and compilers, and to develop models of such complex relationships. These learned models will be used in a variety of tasks such as architecture and application specific program optimizations during compile-time and run-time, and for resource characterization of target architectures. The aim of this sub-project is to produce a machine learning system which would automatically “tune” compilers to new architectures and therefore help provide high performance of applications across a wide range of new and old systems.