

William N. Scherer III

Curriculum vitæ

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PERSONAL DATA

Year of Birth: 1971
Place of Birth: Baltimore, Maryland, USA
Citizenship: USA
Married, two children

EDUCATION

Ph.D. in Computer Science: University of Rochester, Rochester, NY
March 2006
Advisor: Michael L. Scott
M.S. in Computer Science: University of Rochester, Rochester, NY
March 2002
Advisor: Michael L. Scott
B.A. in Computer Science: Carleton College, Northfield, MN
June 1993
Advisor: Richard W. Nau

EMPLOYMENT HISTORY

July 2006-Present: Research Scientist at Rice University
March 2006-July 2006: Postdoc at the University of Rochester
Fall 2002-March 2006: Research Assistant at the University of Rochester
Summer 2002: Intern, Scalable Synchronization Research Group
Sun Microsystems, Burlington, MA
Fall 2001-Spring 2002: Teaching Assistant at the University of Rochester
Summer 2001: Research Assistant at the University of Rochester
1994-2000: Advanced Development Engineer (Consultant)
Vanteon Corporation, Rochester, NY

PUBLICATIONS

1. G. Jin, L. Adhianto, J. Mellor-Crummey, W. N. Scherer III, and C. Yang. Implementation and Performance Evaluation of the HPC Challenge Benchmarks in Coarray Fortran 2.0. To appear in *25th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2011)*, May 2011.
2. W. N. Scherer III, L. Adhianto, G. Jin, J. Mellor-Crummey, and C. Yang. Hiding Latency in Coarray Fortran 2.0. In *4th Conference on Partitioned Global Address Space (PGAS) Programming Models (PGAS 2010)*, October 2010.

3. J. Mellor-Crummey, L. Adhianto, W. N. Scherer III, and G. Jin. A New Vision for Coarray Fortran. In *3rd Conference on Partitioned Global Address Space (PGAS) Programming Models* (PGAS 2009), October 2009
4. J. Shirako, D. M. Peixotto, V. Sarkar, and W. N. Scherer III. Phaser accumulators: A new reduction construct for dynamic parallelism. In *23rd IEEE International Parallel and Distributed Processing Symposium* (IPDPS 2009), May 2009.
5. W. N. Scherer III, D. Lea, and M. L. Scott. Scalable Synchronous Queues. In *Communications of the ACM*, May 2009.
6. R. Zhang, Z. Budlimić, and W. N. Scherer III. Commit Phase in Timestamp-based STM. *20th ACM Symposium on Parallelism in Algorithms and Architectures* (SPAA 2008), Munich, Germany, June 2008. Expanded version available as Technical Report TR08-02, Jan. 2008.
7. J. Mellor-Crummey, L. Adhianto, and W. Scherer. A Critique of Co-array Features in Fortran 2008 Working Draft J3/07-007r3. Paper J3 08-126 of the Fortran 2008 J3 standard working group, at <http://www.j3-fortran.org/doc/meeting/183/08-126.pdf>. February 2008.
8. R. Zhang, Z. Budlimić, M. Joyner, and W. N. Scherer III. Runtime Tuning of STM Validation Techniques. In *Workshop on Exploiting Parallelism with Transactional Memory and other Hardware Assisted Methods* (EPHAM 2008). April 2008.
9. J. Shirako, D. M. Peixotto, V. Sarkar, and W. N. Scherer III. Phasers: a Unified Deadlock-Free Construct for Producer-Consumer and Barrier Synchronization. In *22nd ACM International Conference on Supercomputing* (ICS 2008), Island of Kos, Greece, June 2008.
10. R. Zhang, Z. Budlimić, and W. N. Scherer III. Inside Time-based Software Transactional Memory. Technical Report TR07-5, Rice University, Jul. 2007.
11. T. Bai, X. Shen, C. Zhang, W. N. Scherer III, C. Ding, and M. L. Scott. A Key-Based Adaptive Transactional Memory Executor. NSF Next Generation Software Program Workshop, Mar. 2007. Expanded version available as Technical Report 909, Computer Science Department, University of Rochester, Dec. 2006.
12. W. Scherer. Synchronization and Concurrency in User-level Software Systems. PhD Thesis, University of Rochester, March 2006.
13. M. F. Spear, V. J. Marathe, W. N. Scherer III, and M. L. Scott. Conflict Detection and Validation Strategies for Software Transactional Memory. In *20th Intl. Symp. on Distributed Computing* (DISC 2006), Stockholm, Sweden, Sept. 2006.
14. V. J. Marathe, M. F. Spear, C. Heriot, A. Acharya, D. Eisenstat, W. N. Scherer III, and M. L. Scott. Lowering the Overhead of Nonblocking Software Transactional Memory. In *First ACM SIGPLAN Workshop on Languages, Compilers, and Hardware Support for Transactional Computing* (TRANSACT 2006), Ottawa, Canada, June 2006. An expanded version appears as Technical Report URCS-TR893, Department of Computer Science, University of Rochester, March 2006.
15. A. Shriraman, V. J. Marathe, S. Dwarkadas, M. L. Scott, D. Eisenstat, C. Heriot, W. N. Scherer III, and M. F. Spear. Hardware Acceleration of Software Transactional Memory. In *First ACM SIGPLAN Workshop on Languages, Compilers, and Hardware Support for Transactional Computing* (TRANSACT 2006), Ottawa, Canada,

June 2006. An expanded version appears as Technical URCS-TR887, Department of Computer Science, University of Rochester, March 2006.

16. W. N. Scherer III, D. Lea, and M. L. Scott. Scalable Synchronous Queues. **Winner: Best Student Paper Award.** In *11th ACM Symposium on Principles and Practice of Parallel Programming* (PPoPP 2006), Manhattan, NY, March 2006.
17. S. Heller, M. Herlihy, V. Luchangco, M. Moir, N. Shavit, and W. N. Scherer III. A Lazy Concurrent List-Based Set Algorithm. In *9th International Conference of Principles of Distributed Systems* (OPODIS 2005), Pisa, Italy, December 2005.
18. W. N. Scherer III, D. Lea, and M. L. Scott. A Scalable Elimination-based Exchange Channel. In *OOPSLA Workshop on Synchronization and Concurrency in Object Oriented Languages* (SCOOL 2005) held in conjunction with the *20th ACM Symp. on Object-Oriented Programming, Systems, Languages and Applications* (OOPSLA 2005), San Diego, CA, October 2005.
19. V. J. Marathe, W. N. Scherer III, and M. L. Scott. Adaptive Software Transactional Memory. In *18th Annual Conference on Distributed Computing* (DISC 2005), Cracow, Poland, September, 2005. An earlier version appears as Technical Report URCS-TR868, Department of Computer Science, University of Rochester, May 2005.
20. B. He, W. N. Scherer III, and M. L. Scott. Preemption Adaptivity in Time-Published Queue-Based Spin Locks. In *12th Annual IEEE International Conference on High Performance Computing* (HiPC 2005), Goa, India, December 2005. **Winner: Best Paper Award.** An earlier version appears as Technical Report URCS-TR867, Department of Computer Science, University of Rochester, May 2005.
21. W. N. Scherer III and M. L. Scott. Advanced Contention Management for Dynamic Software Transactional Memory. In *24th ACM Symposium on Principles of Distributed Computing* (PODC 2005), Las Vegas, NV, July 2005.
22. W. N. Scherer III and M. L. Scott. Randomization in STM Contention Management (poster paper; **winner: Most Popular Poster Presentation Award**). In *24th ACM Symposium on Principles of Distributed Computing* (PODC 2005), Las Vegas, NV, July 2005.
23. V. J. Marathe, W. N. Scherer III, and M. L. Scott. Design Tradeoffs in Modern Software Transactional Memory Systems. In *7th Workshop on Languages, Compilers, and Run-time Support for Scalable Systems* (LCR 2004), Houston, TX, October 2004.
24. W. N. Scherer III and M. L. Scott. Nonblocking Concurrent Objects with Condition Synchronization. In *18th Annual Conference on Distributed Computing* (DISC 2004), Amsterdam, The Netherlands, October 2004.
25. W. N. Scherer III and M. L. Scott. Contention Management in Dynamic Software Transactional Memory. In *PODC Workshop on Concurrency and Synchronization in Java Programs* (CSJP 2004) held with the *23rd ACM Symposium on Principles of Distributed Computing* (PODC 2004), St. Johns, NL, Canada, July 2004.
26. M. P. Herlihy, V. Luchangco, M. Moir, and W. N. Scherer III. Software Transactional Memory for Supporting Dynamic-Sized Data Structures. In *22nd ACM Symposium on Principles of Distributed Computing* (PODC 2003), Boston, MA, July 2003.

27. M. L. Scott and W. N. Scherer III. Scalable Queue-Based Spin Locks with Timeout. In *8th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP 2001)*, Snowbird, UT, June 2001.

PRESENTATIONS AND INVITED TALKS

1. Hiding Latency in Coarray Fortran 2.0. *4th Conference on Partitioned Global Address Space (PGAS) Programming Models (PGAS 2010)*. New York, NY, October 2010.
2. CAF 2.0: A Next-generation Co-array Fortran. *International Workshop on Peta-Scale Computing Programming Environment, Languages and Tools (WPSE 2009)*. Tsukuba, Japan, March 2009.
3. Optimization of Timestamp- based Software Transactional Memories. University of Manchester, Manchester, UK, June 2008.
4. High-performance Synchronization for User-level Software Systems. IBM Research, Yorktown, NY, April 2007.
5. High-performance Multithreaded Producer-consumer Designs – from Theory to Practice. Copresented with Doug Lea. Rochester Java Users Group, Rochester, NY, April 2006.
6. Scalable Synchronous Queues. *11th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP 2006)*, Manhattan, NY, March 2006.
7. A Scalable Elimination-based Exchange Channel. *OOPSLA Workshop on Synchronization and Concurrency in Object Oriented Languages (SCOOL 2005)*, San Diego, CA, October 2005.
8. Advanced Contention Management for Dynamic Software Transactional Memory. *24th ACM Symposium on Principles of Distributed Computing (PODC 2005)*, Las Vegas, NV, July 2005.
9. Nonblocking Concurrent Data Structures with Condition Synchronization. Microsoft Research, Cambridge, England, UK, October 2004.
10. Nonblocking Concurrent Objects with Condition Synchronization. *18th Annual Conference on Distributed Computing (DISC 2004)*, Amsterdam, The Netherlands, October 2004.
11. Contention Management in Dynamic Software Transactional Memory. *PODC Workshop on Concurrency and Synchronization in Java Programs (CSJP 2004)*, St. Johns, NL, Canada, July 2004.
12. Practical Issues for Working with Obstruction-Free Software Transactional Memory. *Scalable Synchronization Research Summit*, Sun Microsystems, Burlington, MA, August 2002.

PATENT

1. D. Dice, M. Moir, and W. N. Scherer III. Quickly Reacquirable Locks. U.S. Patent number 7,814,488.

PROFESSIONAL ACTIVITIES

1. Member of the Program Committee for *14th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming* (PPoPP 2009), Raleigh, NC, February 2009.
2. Member of the Program Committee for the TRANSACT 2007 workshop, help in conjunction with *26th Annual ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing* (PODC 2007), Portland, Oregon, Aug. 2007.
3. Named as one of seven full members of the Java Community Process Expert Group on Concurrency (formerly JSR 166), July 2005.
4. Reviewer for journals, conferences, and workshops including: TOCS, TPDS, JPDC, Distributed Computing, ASCA, ICDCS, ICPP, IPDPS, ISPASS, MICRO, PLDI, PODC, PPoPP, SC, SCOOOL