

Features

- Single-speed 1-gigabit/second Ethernet Media Access Controller (MAC)
- Designed to IEEE 802.3-2002 specification
- Reconciliation sublayer with optional GMII
- Optional Full-Duplex Physical Coding Sublayer (PCS) for 1000BASE-X with Ten-Bit Interface (TBI) in the Virtex-II and Spartan-3 families
- Optional Full-Duplex Physical Coding Sublayer (PCS) with Physical Medium Attachment (PMA) for 1000BASE-X in the Virtex-II Pro family
- Configurable Half Duplex and Full Duplex operation with GMII in the Virtex-II family
- Configured and monitored through an independent microprocessor-neutral interface
- Powerful statistics gathering to internal counters (statistic vectors are also output externally for user access)
- Configurable flow control through MAC Control pause frames; symmetrically or asymmetrically enabled
- Optional MDIO interface to managed objects in PHY layers (MII Management)
- Support of VLAN frames to specification IEEE 802.3-2002
- Configurable support of *jumbo frames* of any length
- Configurable inter frame gap adjustment
- Configurable in-band FCS field passing on both transmit and receive paths
- Optional PCS supports Auto-Negotiation for information exchange with a link partner
- Available under terms of the SignOnce IP License



LogiCORE™ Facts

Core Specifics

Supported Family (GMII configuration)	Virtex™-E (-7) Virtex-II™ (-4) Virtex-II Pro™ (-5) Spartan™-IIE (-7) Spartan-3 (-4)
Supported Family (1000BASE-X PCS with TBI configuration)	Virtex-II (-4) Virtex-II Pro(-5) Spartan-3 (-4)
Supported Family (1000BASE-X PCS & PMA configuration)	Virtex-II Pro(-5)
Performance	125 MHz internal clock;
Size	581 - 1850 slices
Global Clock Buffers	2 - 4

Provided with Core

Documentation	Product Specification
Design File Formats	EDIF and NGC netlist, HDL wrapper
Constraints File	UCF

Design Tools Requirements

Xilinx Core Tools	v6.1i SP3
-------------------	-----------

Support

Provided by Xilinx

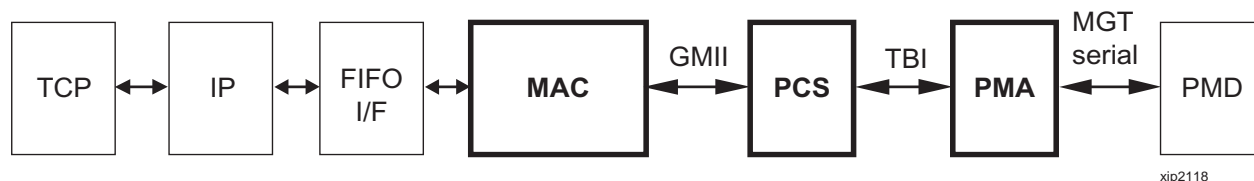


Figure 1: Typical Gigabit Ethernet Architecture

© 2003 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and further disclaimers are as listed at <http://www.xilinx.com/legal.htm>. All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.

NOTICE OF DISCLAIMER: Xilinx is providing this design, code, or information "as is." By providing the design, code, or information as one possible implementation of this feature, application, or standard, Xilinx makes no representation that this implementation is free from any claims of infringement. You are responsible for obtaining any rights you may require for your implementation. Xilinx expressly disclaims any warranty whatsoever with respect to the adequacy of the implementation, including but not limited to any warranties or representations that this implementation is free from claims of infringement and any implied warranties of merchantability or fitness for a particular purpose.

MAC Overview

The 1-Gigabit Ethernet MAC is part of the Ethernet architecture displayed in [Figure 1](#). The part of this architecture from the MAC to the right is defined in specification IEEE 802.3-2002.

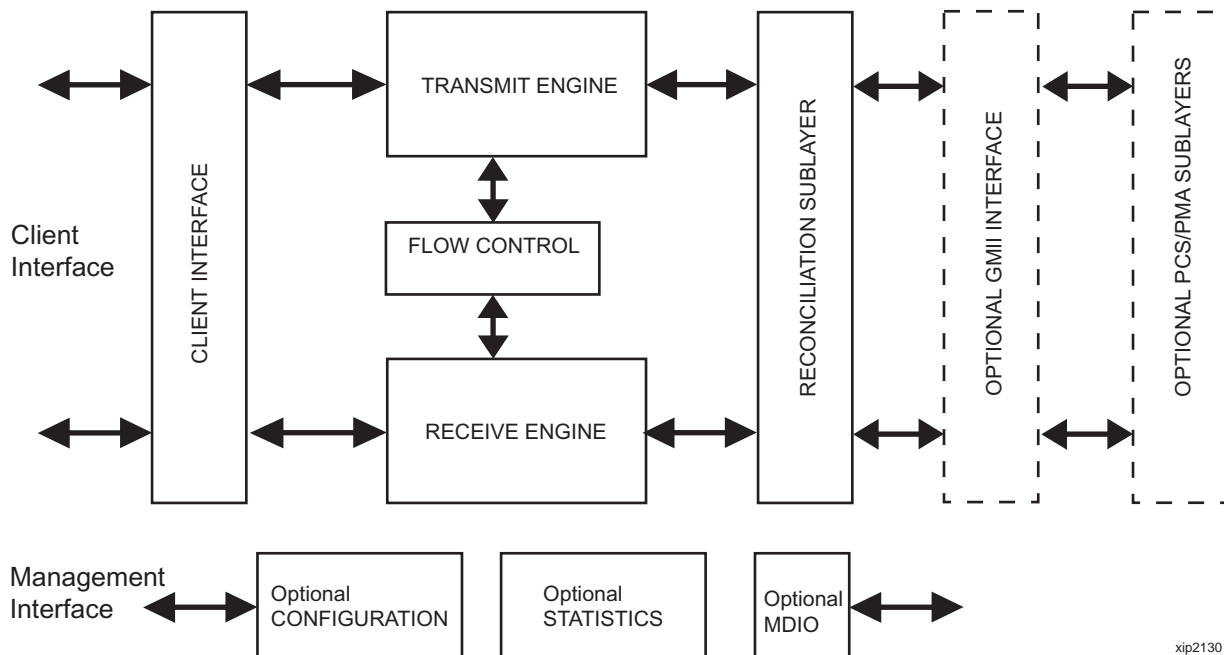
A block diagram of the MAC core is displayed in [Figure 2](#), which shows the major functional blocks of the MAC:

- Client interface
- Transmit engine
- Flow control block
- Receive engine
- Reconciliation sublayer (RS)
- Optional management interface and MDIO
- Optional statistics block
- Optional GMII interface
- Optional PCS/PMA sublayers for 1000BASE-X

The client interface has fully independent 8-bit interfaces for both transmit and receive to support full-duplex operation.

Configuration of the core, access to the statistics block and access to the MDIO port are accessed through the optional management interface, a 32 bit processor-neutral data pathway that is independent of the Ethernet data pathway. When the management interface is omitted, configuration of the core can still be made via an alternative configuration vector.

The Gigabit Media Independent Interface (GMII) is the interface available to all supported device families. In the Virtex-II family, the GMII can be replaced by a 1000BASE-X PCS with Ten Bit Interface (TBI). In the Virtex-II Pro family, the GMII or TBI can be replaced with 1000BASE-X PCS and PMA sublayers; this uses the Rocket I/O™ Multi-Gigabit Transceiver (MGT) technology to transmit and receive 1.25 Gbp/s serial data over differential lines



xip2130

Figure 2: Functional Block Diagram of the 1 Gigabit Ethernet MAC

Xilinx CORE Generator

The 1-Gigabit Ethernet MAC Core is generated through the Xilinx CORE Generator™ system. The following sections describe the graphical user interface (GUI) options and the generated output files.

GUI Interface

Component Name

The component name is used as the base name of the output files generated for the core. Names must begin with a letter and must be composed from the following characters: a through z, 0 through 9 and “_”.

Half Duplex Capable

Select this option to have the MAC work in both full-duplex and half-duplex modes, select the Half Duplex Capable option.

The default is half-duplex capability. Note that half-duplex capability is not supported in the Virtex-E or Spartan-IIE families.

Management Interface

Select this option if you wish to include the optional Management Interface (see [page 30](#)). If this option is not selected, the core will be generated with a configuration vector.

The default is to have the management interface.

Statistics Gathering

Select this option to include the optional Statistical Gathering with the core (see [page 34](#)). This option is available only if the core includes the optional management interface. The statistics vectors are available whether or not this option is selected.

The default is to gather statistics.

Memory Type

If the statistics gathering option is selected, it is possible to choose which memory type the statistics are stored in. The choices are *Block Memory* or *Distributed Memory*. The choice of these should be based on the availability of resources in your design. There is no performance or functional difference between the memory types.

The default type is the *Block Memory*. Note that *Distributed Memory* is not supported in the Virtex-E or Spartan-IIE families.

Physical Interface

Depending on the target Xilinx FPGA architecture, it may be possible to select from three different physical interface choices for the core:

- GMII - see the optional GMII on [page 40](#)
- TBI - see the optional PCS on [page 43](#)
- PHY - see the optional PCS & PMA sublayers on [page 46](#)

The *TBI* option is not supported in the Virtex-E or Spartan-IIE families. The *PHY* option is supported in the Virtex-II Pro family only.

The default is the *GMII* physical interface.

Parameter Values in the XCO File

XCO file parameter names and their values are identical to the names and values shown in the GUI, except that underscore characters () are used instead of spaces. The text in an XCO file is case insensitive.

Table 1 shows the XCO file parameters and values, and summarizes the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET component_name = abc123
CSET physical_interface = gmii
CSET statistics_gathering = true
CSET half_duplex_capable = true
CSET memory_type = block_memory
CSET management_interface = true
```

Table 1: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _	blank
physical_interface	One of the following keywords: gmii, tbi, phy	gmii
statistics_gathering	One of the following keywords: true, false	true
half_duplex_capable	One of the following keywords: true, false	true
memory_type	One of the following keywords: block_memory, distributed_memory	block_memory
management_interface	One of the following keywords: true, false	true

Output Generation

The output files generated from the CORE Generator are placed in the CORE Generator project directory. The output files include: two netlist files, supporting CORE Generator files, a readme file and a subdirectory containing example wrapper files and scripts to take the core through the Xilinx implementation software and simulate the core using the

Modelsim simulator by Model Technology. See the generated readme files for explanations about these files.

Device Utilization

Table 2 provides approximate slice counts for the core's various options when instantiated in a Virtex-II Pro device.

Table 2: Device Utilization

Parameter Values							Device Resources				
Physical Interface			Half Duplex	Management Interface	Statistics Gathering		Slices	LUT	Registers	BRAM	GCLK
GMII	TBI	PHY			Distributed Memory	Block Memory					
Yes	No	No	Yes	Yes	Yes	No	1545	2159	1654	0	3
Yes	No	No	Yes	Yes	No	Yes	1420	1745	1561	2	3
Yes	No	No	Yes	Yes	No	No	932	1140	991	0	3
Yes	No	No	Yes	No	No	No	781	969	831	0	2
Yes	No	No	No	Yes	Yes	No	1315	1752	1359	0	3
Yes	No	No	No	Yes	No	Yes	1159	1525	1317	2	3
Yes	No	No	No	Yes	No	No	742	884	793	0	3
Yes	No	No	No	No	No	No	581	708	630	0	2
No	Yes	No	No	Yes	Yes	No	1850	2345	1934	2	4
No	Yes	No	No	Yes	No	Yes	1697	1880	1899	4	4
No	Yes	No	No	Yes	No	No	1295	1404	1380	2	4
No	Yes	No	No	No	No	No	1122	1226	1213	2	3
No	No	Yes	No	Yes	Yes	No	1725	1773	1791	0	3
No	No	Yes	No	Yes	No	Yes	1580	1838	1775	2	3
No	No	Yes	No	Yes	No	No	1172	1394	1236	0	3
No	No	Yes	No	No	No	No	1005	1183	1066	0	2

1. Half Duplex Logic is only available with the GMII.
2. Statistics Gathering is only available when the Management Interface is selected

Interface Description

All ports of the core (with the exception of the Rocket I/O serial ports of the optional PCS/PMA sublayers) are internal connections in FPGA fabric. An example wrapper is delivered with the core which adds IBUFs, OBUFs and IOB flip-flops where appropriate to the external signals of the GMII or TBI. IOBs are also added to the remaining unconnected ports to allow the example design to be taken

through the Xilinx implementation software. In addition, all clock management logic is placed in this example wrapper; this allows the user more flexibility in implementation, for example, in designs using multiple cores.

The example wrapper is provided in both VHDL and Verilog.

Interface Signals for MAC with `physical_interface=gmii` and `management_interface=true`

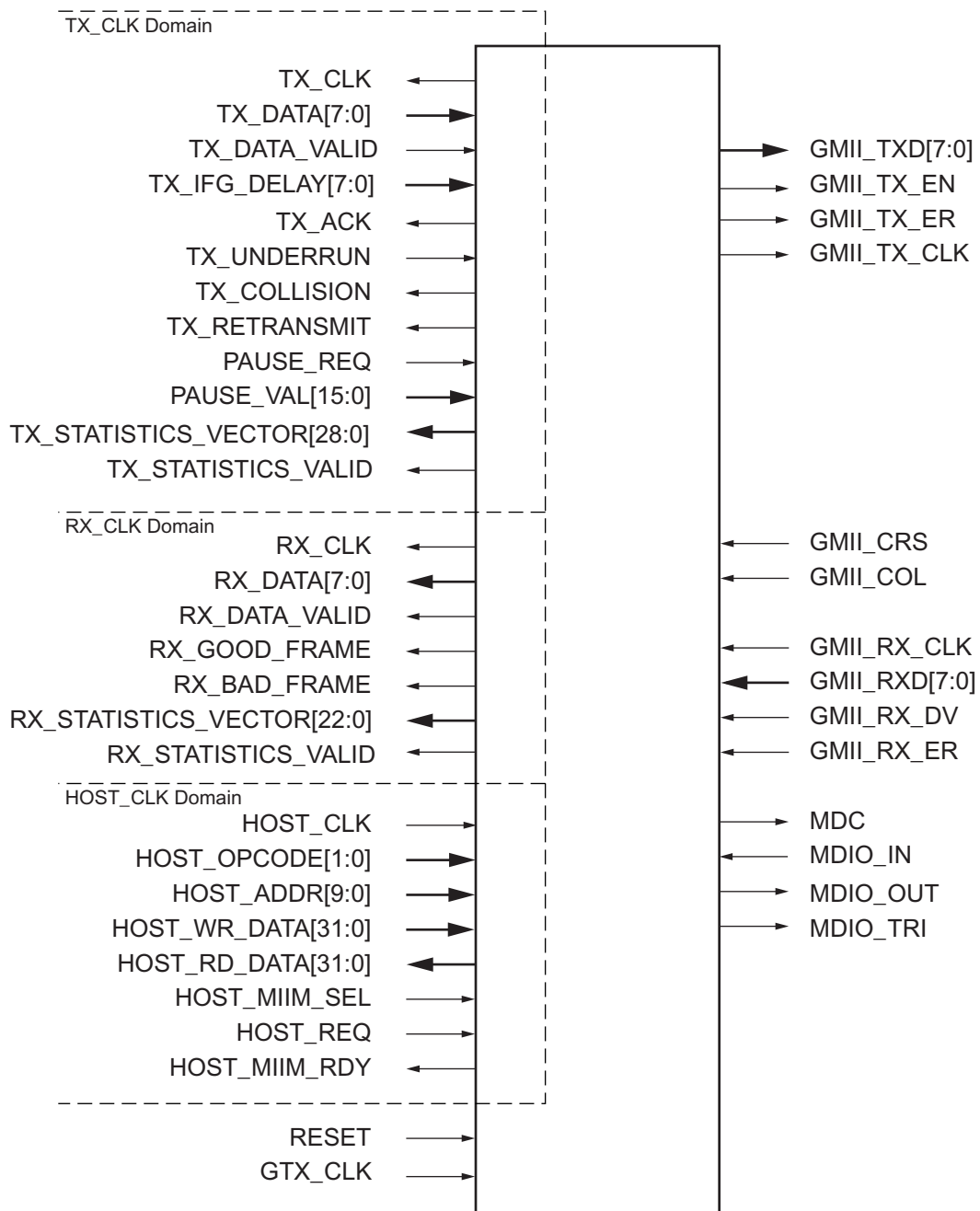


Figure 3: Component Pinout for MAC with GMII Interface using the optional Management Interface

Interface Signals for MAC with `physical_interface=gmii` and `management_interface=false`

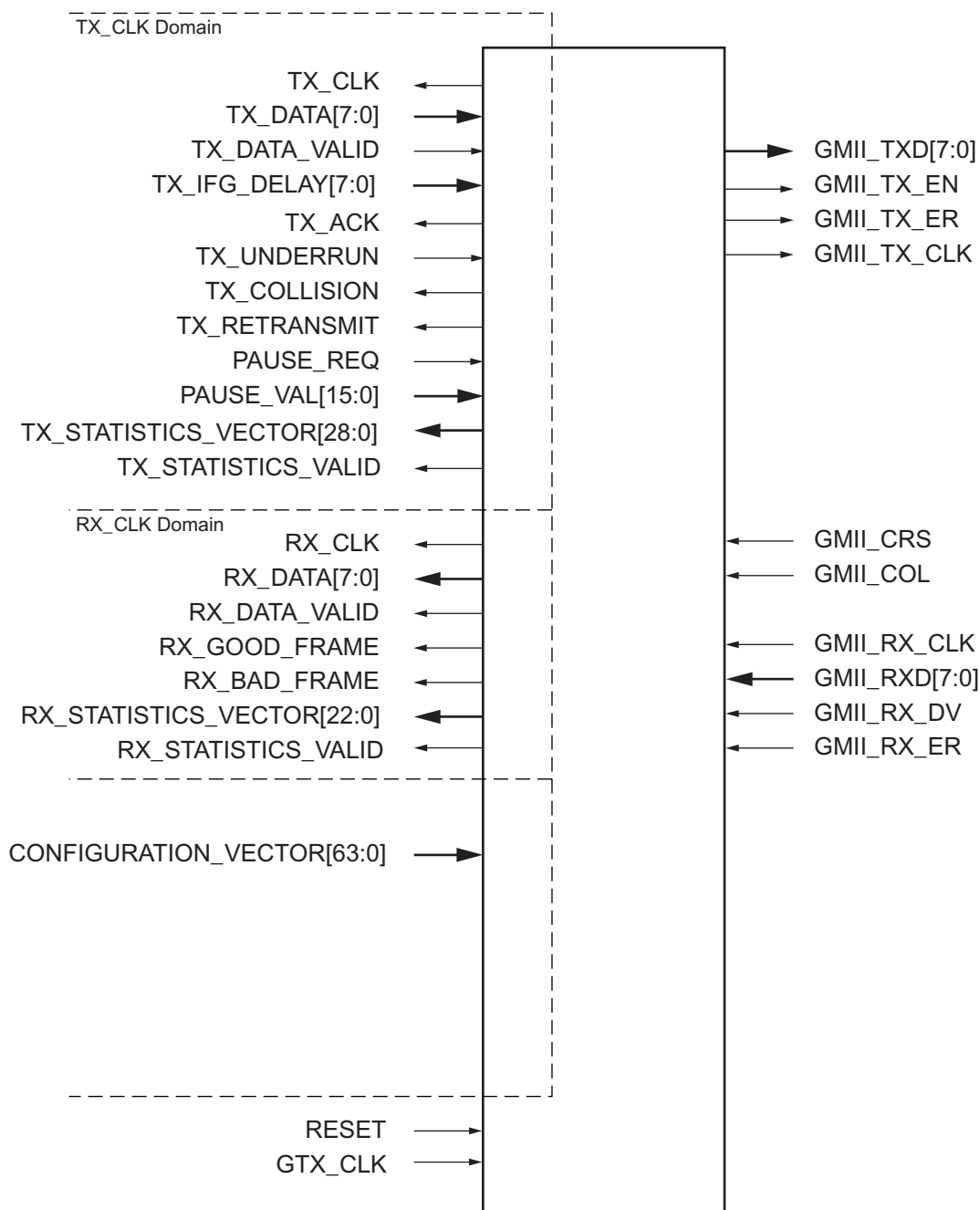


Figure 4: Component Pinout for MAC with GMII Interface without the optional Management Interface

Interface Signals for MAC with `physical_interface=tbi` and `management_interface=true`

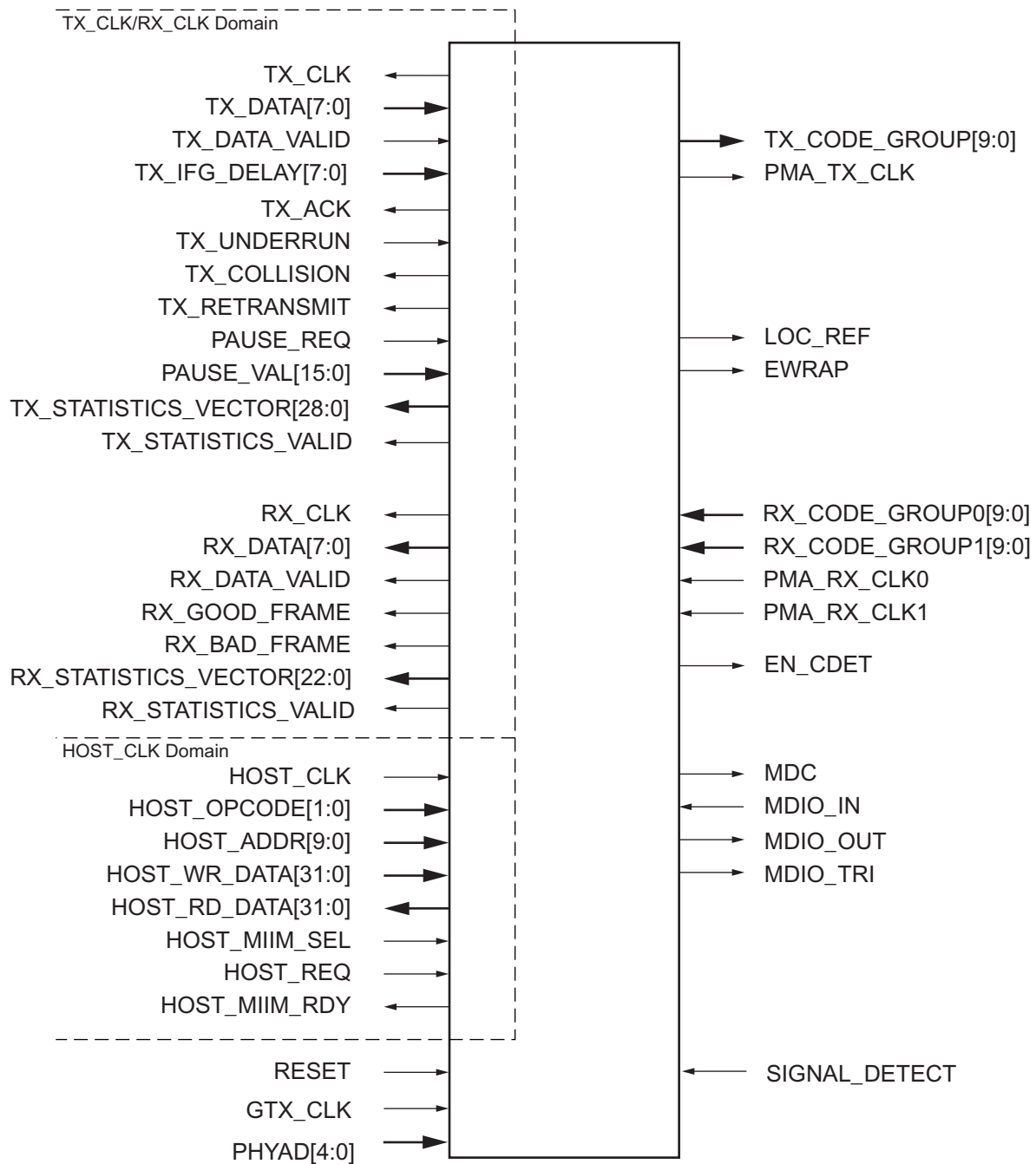


Figure 5: Component Pinout for MAC with PCS and TBI using the optional Management Interface

Interface Signals for MAC with `physical_interface=tbi` and `management_interface=false`

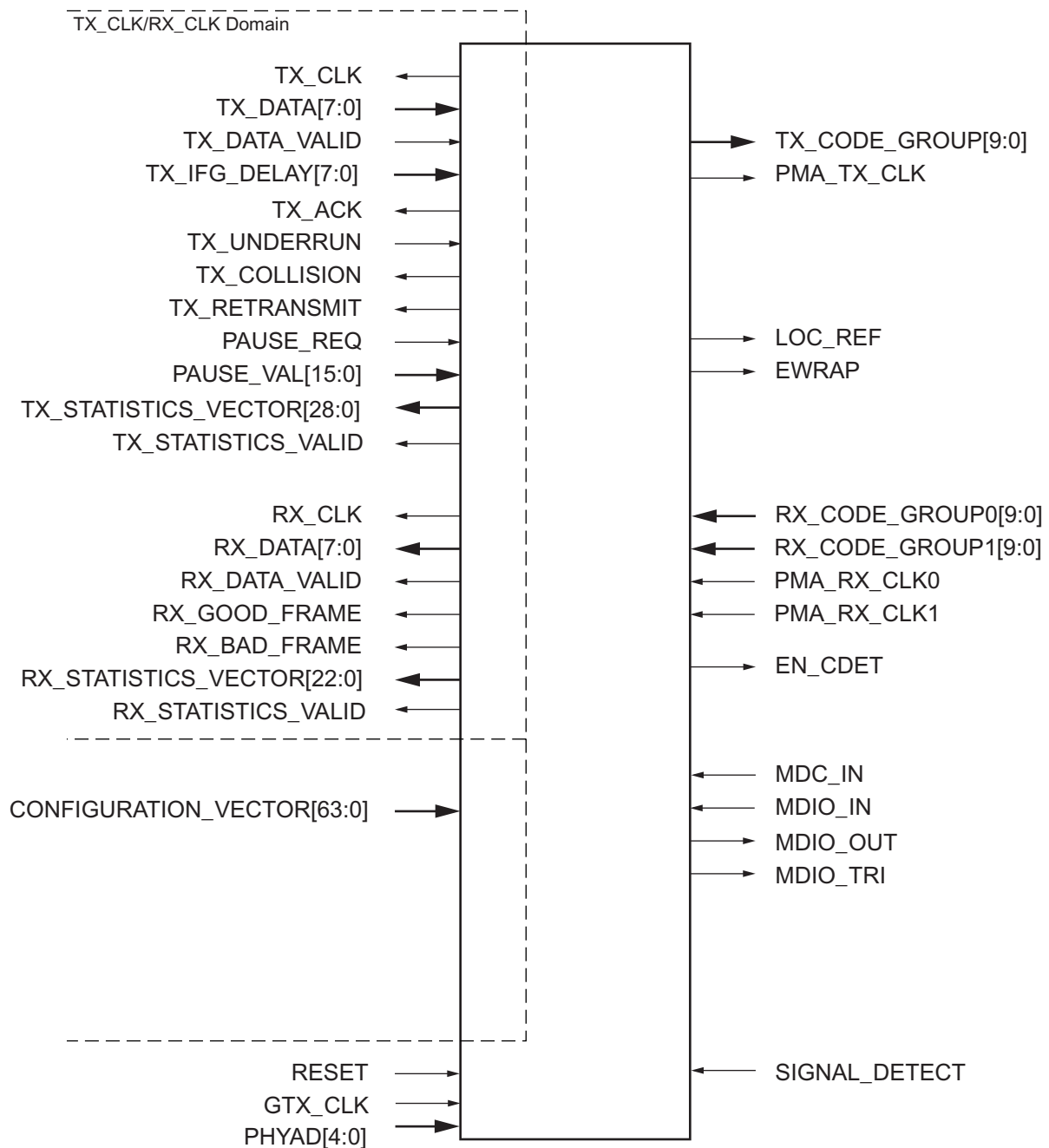


Figure 6: Component Pinout for MAC with PCS and TBI without the optional Management Interface

Interface Signals for MAC with `physical_interface=phy` and `management_interface=true`

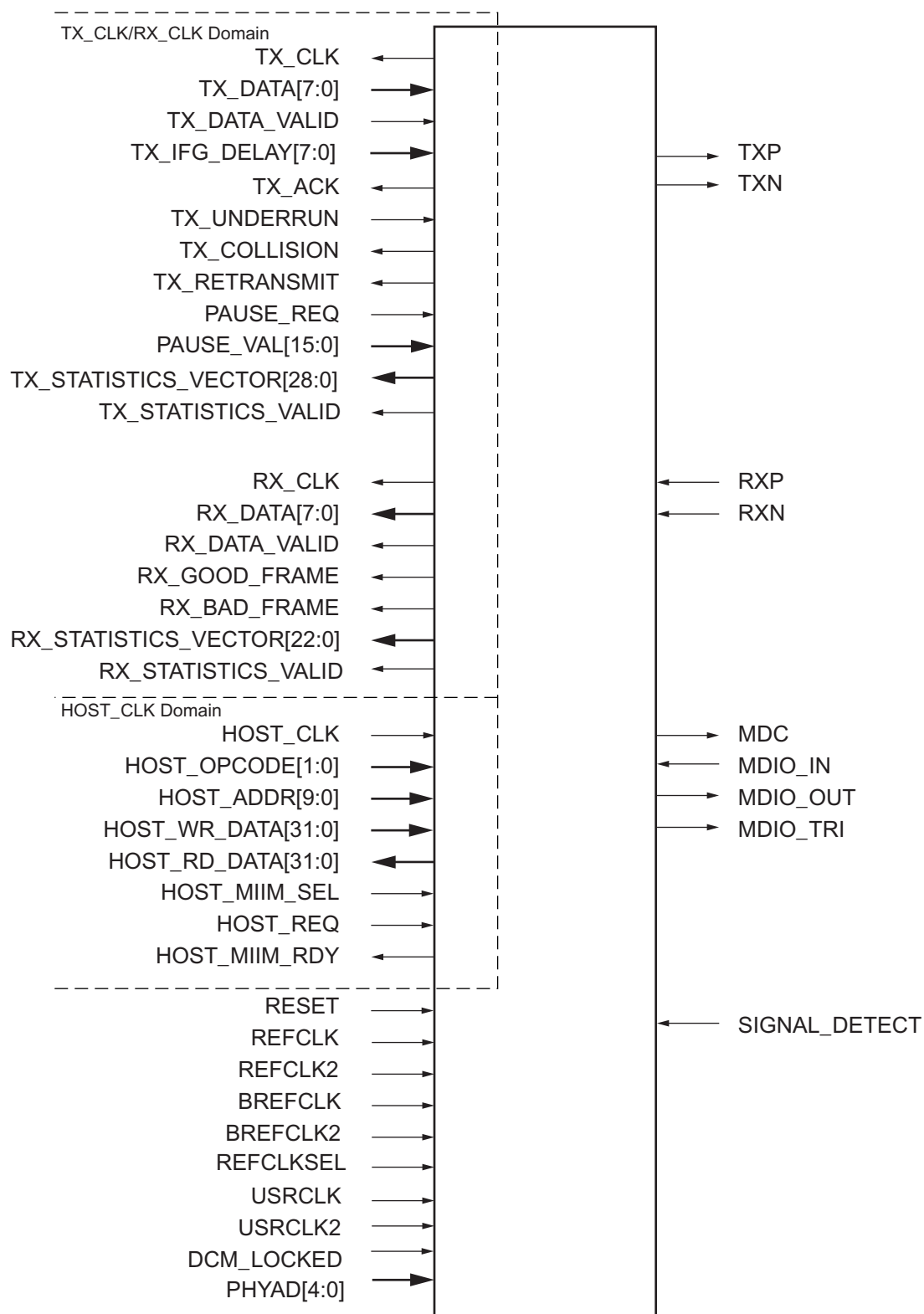


Figure 7: Component Pinout for MAC with PCS & PMA Sublayers using the optional Management Interface

Interface Signals for MAC with `physical_interface=phy` and `management_interface=false`

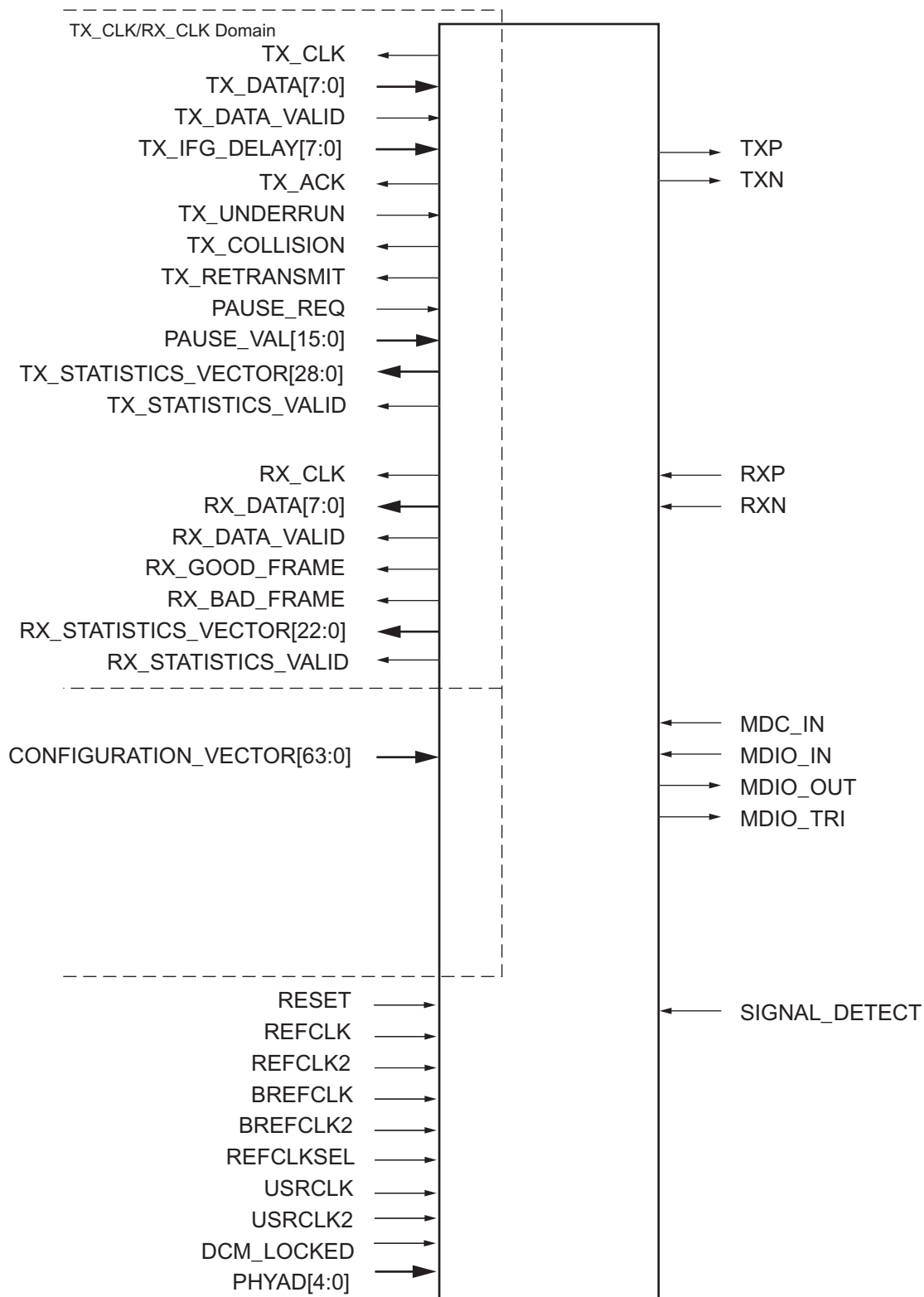


Figure 8: Component Pinout for MAC with PCS & PMA Sublayers without the optional Management Interface

Client Side Interface Signal Definition

Table 3 describes the client-side transmit signals of the MAC core. These signals are used to transmit data from the client to the MAC core.

Table 3: Transmit Client Interface Signal Pins

Signal	Direction	Description
TX_CLK	Output	Clock for transmit client interface. 125 MHz nominal.
TX_DATA[7:0]	Input	Frame data to be transmitted is supplied on this port.
TX_DATA_VALID	Input	Control signal for TX_DATA port.
TX_IFG_DELAY[7:0]	Input	Control signal for configurable Inter Frame Gap adjustment. See "Transmitter" on page 16 for timing diagrams.
TX_ACK	Output	Handshaking signal. Asserted when the current data on TX_DATA has been accepted. See "Transmitter" on page 16 for timing diagrams.
TX_UNDERRUN	Input	Asserted by client to force MAC core to corrupt the current frame.
TX_COLLISION	Output	Asserted by the MAC core to signal a collision on the medium and that any transmission in progress should be aborted. Always 0 when the MAC core is in full-duplex mode.
TX_RETRANSMIT	Output	When asserted at the same time as the TX_COLLISION signal, this signals the client that the aborted frame should be resupplied to the MAC core for retransmission. Always 0 when the MAC core is in full-duplex mode.
TX_STATISTICS_VECTOR[28:0]	Output	This gives information on the last frame transmitted. See "Transmitter" on page 16 for vector contents.
TX_STATISTICS_VALID	Output	Asserted at end of frame transmission, indicating that the TX_STATISTICS_VECTOR is valid.

Notes:

1. All the above signals are synchronous to TX_CLK and Active High.

Table 4 describes the client-side receive signals. These signals are used by the MAC core to transfer data to the client.

Table 4: Receive Client Interface Signal Pins

Signal	Direction	Description
RX_CLK	Output	Clock for receive client interface. 125 MHz nominal.
RX_DATA[7:0]	Output	Frame data received is supplied on this port.
RX_DATA_VALID	Output	Control signal for the RX_DATA port.
RX_GOOD_FRAME	Output	Asserted at end of frame reception to indicate that the frame should be processed by the MAC client. See "Receiver" on page 24
RX_BAD_FRAME	Output	Asserted at end of frame reception to indicate that the frame should be discarded by the MAC client. See "Receiver" on page 24
RX_STATISTICS_VECTOR[22:0]	Output	Provides information about the last frame received. See "Receiver" on page 24 for the vector contents.
RX_STATISTICS_VALID	Output	Asserted at end of frame reception, indicating that the RX_STATISTICS_VECTOR is valid.

Notes:

1. All signals above are synchronous to RX_CLK and Active High.

Table 5 describes the signals used by the client to request a flow control action from the transmit engine. Flow control frames received by the MAC are automatically handled (if the MAC is configured to do so).

Table 5: Flow Control Interface Signal Pinout

Signal	Direction	Description
PAUSE_REQ	Input	Pause request: sends a pause frame down the link. See "Transmitting a PAUSE Control Frame" on page 29 .
PAUSE_VAL[15:0]	Input	Pause value: inserted into the parameter field of the transmitted pause frame.

Notes:

1. These signals are synchronous to TX_CLK and are Active High.

Table 6 describes the optional signals used by the client to access the management features of the MAC core, including configuration, status, statistics, and MDIO access.

Table 6: Optional Management Interface Signal Pinout (management_interface=true)

Signal	Direction	Description
HOST_CLK	Input	Clock for management interface. See "Optional Management Interface (management_interface=true)" on page 30 for the signal frequency range.
HOST_OPCODE[1:0]	Input	Defines operation to be performed over MDIO interface. Bit 1 is also used in configuration register access. See "Configuration Registers" on page 30 .
HOST_ADDR[9:0]	Input	Address of register to be accessed.
HOST_WR_DATA[31:0]	Input	Data to write to register.
HOST_RD_DATA[31:0]	Output	Data read from register.
HOST_MIIM_SEL	Input	When asserted, the MDIO interface is accessed. When disasserted, the MAC internal configuration or statistical counter registers are accessed.
HOST_REQ	Input	Used to signal a transaction on the MDIO interface or to read from the statistic registers. See "Optional Management Interface (management_interface=true)" on page 30 .
HOST_MIIM_RDY	Output	When high, the MDIO interface has completed any pending transaction and is ready for a new transaction.

Notes:

1. All signals above are synchronous to HOST_CLK and are Active High.

Table 7 describes the alternative to the optional Management Interface signals. This describes the Configuration Vector which uses direct inputs to the core to replace the functionality of the MAC Configuration bits when the Management Interface is not used..

Table 7: Alternative to the Optional Management Interface: Configuration Vector Signal Pinout (management_interface=false)

Signal	Direction	Description
CONFIGURATION_VECTOR[63:0]	Input	The Configuration Vector is used to replace the functionality of the MAC Configuration Registers when the Management Interface is not used. See "Optional Configuration Vector (management_interface = false)" on page 38 .

Notes:

1. All bits of CONFIGURATION_VECTOR are registered on input but may be treated as asynchronous inputs.

Table 8 describes the reset signal.

Table 8: Reset Signal

Signal	Direction	Description
RESET	Input	Asynchronous reset for entire core. See "Reset circuit" on page 42 for more information on the reset circuit.

Physical Interface Signal Definition

Table 9 describes the MDIO (MII Management) interface signals of the MAC core. These signals are typically connected to the MDIO port of a PHY device, either off-chip or an SoC-integrated core. The MDIO format is defined in IEEE802.3 clause 22.

Table 9: MDIO Interface Signal Pinout

Signal	Direction	Description
MDC	Output	Management Clock: derived from HOST_CLK on the basis of supplied configuration data when the optional Management Interface is used. See "Optional Management Interface (management_interface=true)" on page 30
MDC_IN	Input	When the Optional Management Interface is not used, access to the optional Physical Coding Sublayer (PCS) must be provided by an external MDIO Controller. In this situation the Management Clock is an input to the core.
MDIO_IN	Input	Input data signal for communication with PHY configuration and status. Tie high if unused.
MDIO_OUT	Output	Output data signal for communication with PHY configuration and status.
MDIO_TRI	Output	Tristate control for MDIO signals; 0 signals that the value on MDIO_OUT should be asserted onto the MDIO bus.

Table 10 describes the optional GMII signals of the MAC core. These are typically attached to a PHY module, either off-chip or internally integrated. The GMII is defined in IEEE802.3 clause 35.

Table 10: Optional GMII Interface Signal Pinout (physical_interface=gmii)

Signal	Direction	Description
GTX_CLK	Input	Clock signal at 125 MHz. Other transmit clocks are derived from this clock as illustrated in Figure 28. Tolerance must be within IEEE 802.3-2002 specification.
GMII_TXD[7:0]	Output	Transmit data to PHY.
GMII_TX_EN	Output	Data Enable control signal to PHY.
GMII_TX_ER	Output	Error control signal to PHY.
GMII_TX_CLK	Output	Clock out to PHY.
GMII_CRS	Input	Control signal from PHY.
GMII_COL	Input	Control signal from PHY.
GMII_RX_CLK	Input	Recovered clock from received data stream by PHY.
GMII_RXD[7:0]	Input	Received data from PHY.
GMII_RX_DV	Input	Data Valid control signal from PHY.
GMII_RX_ER	Input	Error control signal from PHY.

Table 11 describes the TBI (Ten-Bit interface) signals of the MAC core. These are typically attached to a PMA SERDES module. These signals optionally replace the GMII signals described in **Table 10** to extend the functionality of the core to include the PCS for 1000BASE-X. The TBI is defined in IEEE802.3 clause 36.

Table 11: Optional TBI Interface Signal Pinout (physical_interface=tbi)

Signal	Direction	Description
GTX_CLK	Input	Clock signal at 125 MHz. Other transmit clocks will be derived from this clock as illustrated in Figure 32 . Tolerance must be within IEEE 802.3-2002 specification.
TX_CODE_GROUP[9:0]	Output	10-bit parallel transmit data to PMA Sublayer (SERDES).
PMA_TX_CLK	Output	Transmit clock signal to PMA Sublayer (SERDES) at 125MHz.
LOC_REF	Output	Causes the PMA sublayer clock recovery unit to lock to PMA_TX_CLK. This signal is tied to Ground.
EWRAP	Output	This signal is set from the PCS Control Register 0, bit 14 (loopback). See " PCS Managed Register Block (physical_interface = tbi or phy) " on page 49. When high this instructs the PMA sublayer to electrically loop the transmitter data to the receiver.
RX_CODE_GROUP0[9:0]	Input	10-bit parallel received data from PMA Sublayer (SERDES); synchronous to PMA_RX_CLK0.
RX_CODE_GROUP1[9:0]	Input	10-bit parallel received data from PMA Sublayer (SERDES); synchronous to PMA_RX_CLK1.
PMA_RX_CLK0	Input	Received clock signal from PMA Sublayer (SERDES) at 62.5MHz.
PMA_RX_CLK1	Input	Received clock signal from PMA Sublayer (SERDES) at 62.5MHz. This is 180 degrees out of phase with PMA_RX_CLK0.
EN_CDET	Output	Enables the PMA Sublayer to perform comma realignment; driven from the PCS state machine during the Loss-Of-Sync state.
PHYAD[4:0]	Input	PHY address of MDIO register set for the PCS.
SIGNAL_DETECT	Input	Signal direct from PMD sublayer indicating the presence of light detected at the optical receiver. If driven high, this indicates that the optical receiver has detected light. If driven low this indicates the absence of light. If unused, tie high to enable the operation the core.

Notes:

PHYAD and SIGNAL_DETECT are asynchronous inputs. SIGNAL_DETECT is Active High.

Table 12 describes the interface signals for the Optional PCS/PMA sublayer of the MAC core. These signals optionally replace the GMII signals described in **Table 10** to extend the functionality of the core to include the PCS and PMA sublayers for 1000BASE-X. This option uses the Virtex-II Pro Rocket I/O functionality which is integrated into the core. The PMA sublayer for 1000BASE-X is defined in IEEE802.3 clause 36.

Table 12: Optional PCS/PMA sublayer Interface Signal Pinout (physical_interface=phy)

Signal	Direction	Description
REFCLK	Input	High Quality Reference clock for Multi-Gigabit Transceivers (62.5 MHz). See Rocket I/O User Guide.
REFCLK2	Input	Alternative High Quality Reference clock for Multi-Gigabit Transceivers (62.5 MHz). See Rocket I/O User Guide.
BREFCLK	Input	Alternative High Quality Reference clock for Multi-Gigabit Transceivers (62.5 MHz). This optionally replaces REFCLK. See Rocket I/O User Guide.
BREFCLK2	Input	Alternative High Quality Reference clock for Multi-Gigabit Transceivers (62.5 MHz). This optionally replaces REFCLK2. See Rocket I/O User Guide.
REFCLKSEL	Input	Selects between either (B)REFCLK or (B)REFCLK2 as the input clock source to the MGT. See Rocket I/O User Guide.
USERCLK	Input	Clock signal at 62.5 MHz. This is connected to the TXUSRCLK and RXUSRCLK ports of the Rocket I/O MGT. This may be derived from (B)REFCLK using a DCM as illustrated in Figure 35 .
USERCLK2	Input	Clock signal at 125 MHz. This is connected to the TXUSRCLK2 and RXUSRCLK2 ports of the Rocket I/O MGT. This may be derived from (B)REFCLK using a DCM as illustrated in Figure 35 .
DCM_LOCKED	Input	If a DCM is used to derive USRCLK and USRCLK2 as illustrated in Figure 35 , the LOCKED port of the DCM must be connected to the DCM_LOCKED port of the core. The core will hold it's Rocket I/O MGT in reset until DCM_LOCKED is driven to logic 1.
TXP/TXN	Output	Differential pair for serial transmission from PMA to PMD. The clock is embedded in the data stream.
RXP/RXN	Input	Differential pair for serial reception from PMD to PMA. The clock is extracted from the data stream.
PHYAD[4:0]	Input	PHY address of MDIO register set for the PCS.
SIGNAL_DETECT	Input	Signal direct from PMD sublayer indicating the presence of light detected at the optical receiver. If driven high, this indicates that the optical receiver has detected light. If driven low this indicates the absence of light. If unused, tie high to enable the operation the core.

Notes:

1. PHYAD and SIGNAL_DETECT are asynchronous inputs. SIGNAL_DETECT is Active High.

Functional Description

Client Interface

The client interface is designed for maximum flexibility in matching to a client switching fabric or network processor interface.

The data pathway is 8 bits wide in both the transmit and receive directions, with each pathway synchronous to the TX_CLK and RX_CLK respectively for completely independent full duplex operation.

Transmitter

Normal Frame Transmission

The timing of a normal outbound frame transfer can be seen in [Figure 9](#). When the client wants to transmit a frame, it places the first column of data onto the TX_DATA port and asserts a “1” onto TX_DATA_VALID.

When the MAC core has read this first byte of data, it will assert the TX_ACK signal; on the next and subsequent rising clock edges, the client must provide the remainder of the data for the frame.

The end of frame is signalled to the MAC core by taking TX_DATA_VALID Low.

In-Band Parameter Encoding

For maximum flexibility in switching applications, the Ethernet frame parameters (destination address, source address, length/type and optionally FCS) are encoded within the same data stream that the frame payload is transferred upon, rather than on separate ports. This is illustrated in the timing diagrams. Definitions of the abbreviations used in the timing diagrams are described in [Table 13](#).

Table 13: Abbreviations Used in Timing Diagrams

Abbreviation	Definition
DA	Destination Address; 6 bytes
SA	Source Address; 6 bytes
L/T	Length/Type Field; 2 bytes
FCS	Frame Check Sequence; 4 bytes

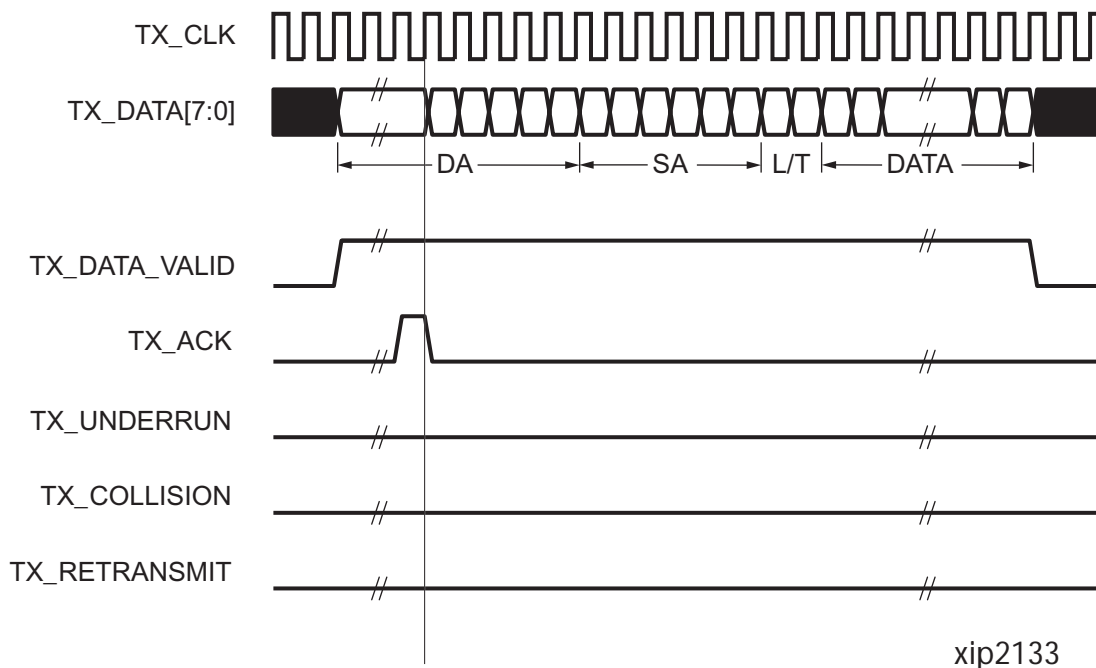


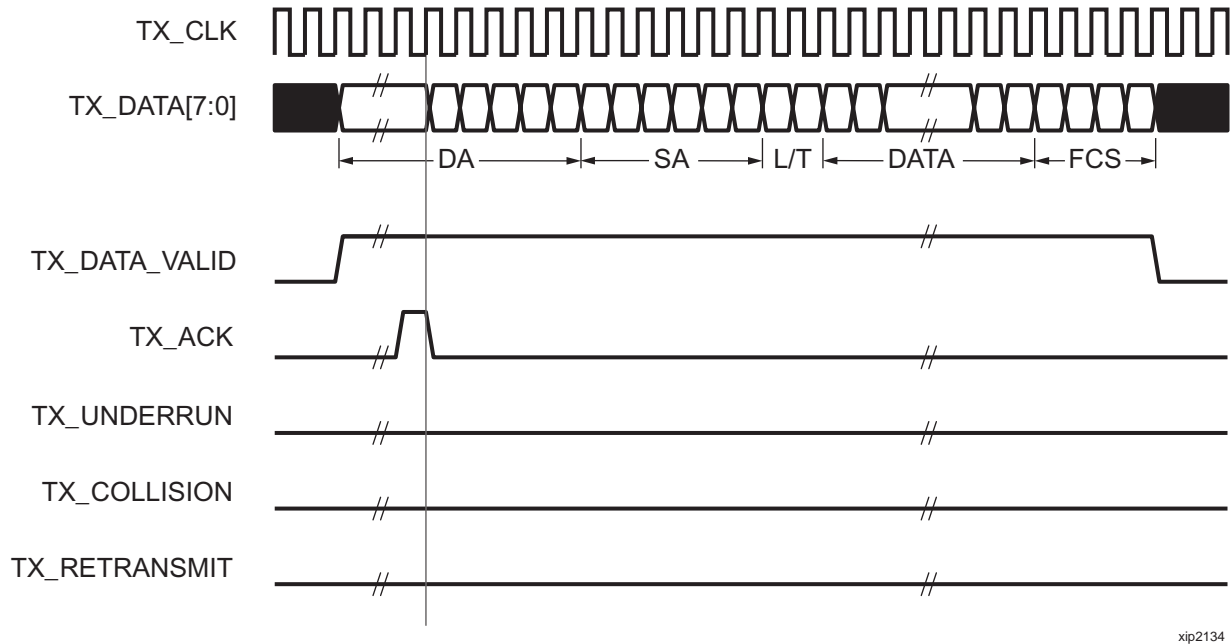
Figure 9: Normal Frame Transmission Across Client Interface

Padding

When fewer than 46 bytes of data are supplied by the client to the MAC core, the transmitter module will add padding up to the minimum frame length. The exception to this is when the MAC core is configured for client-passed FCS; in this case the client must also supply the padding to maintain the minimum frame length (see [Client-Supplied FCS Passing](#)).

Client-Supplied FCS Passing

If the MAC core is configured to have the FCS field passed in by the client (see ["Configuration Registers" on page 30](#)), the transmission timing is as depicted in [Figure 10](#). In this case, it is the responsibility of the client to ensure that the frame meets the Ethernet minimum frame length requirements; the MAC core will not perform any padding of the payload.



xip2134

Figure 10: Frame Transmission with Client-supplied FCS

Client Underrun

The timing of an aborted transfer can be seen in **Figure 11**. This may happen, for instance, if a FIFO connected to the client interface empties before a frame is completed. When the client asserts TX_UNDERRUN during a frame transmission, the MAC core will insert an error code to corrupt the

current frame, and then fall back to idle transmission. It is the responsibility of the client to re-queue the aborted frame for transmission.

When an underrun occurs, TX_DATA_VALID may be asserted on the clock cycle after the TX_UNDERRUN assertion to request a new transmission.

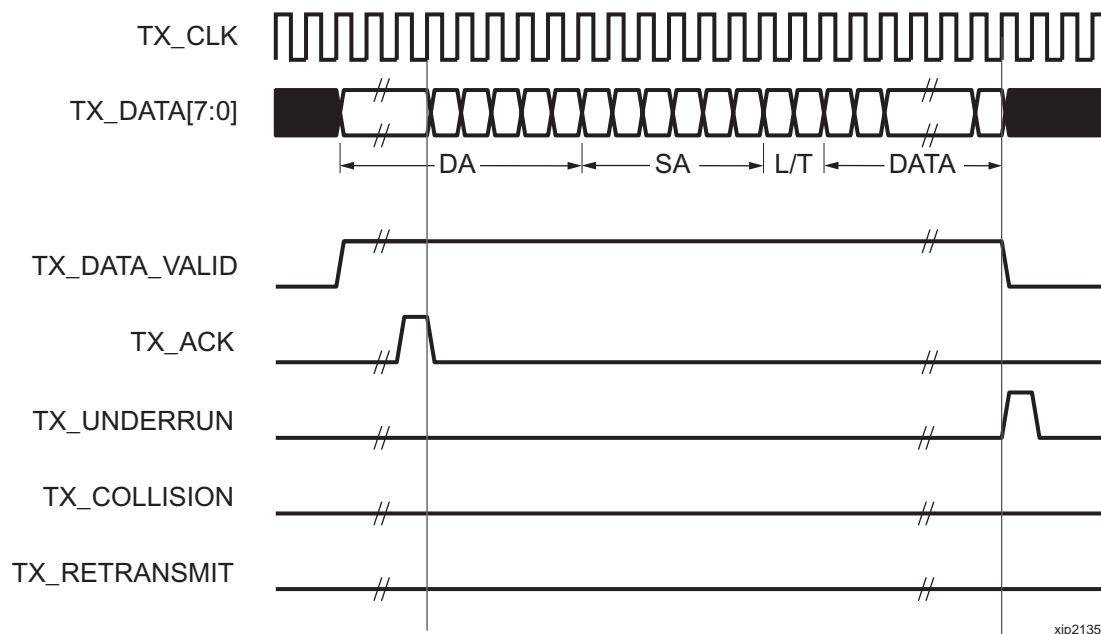


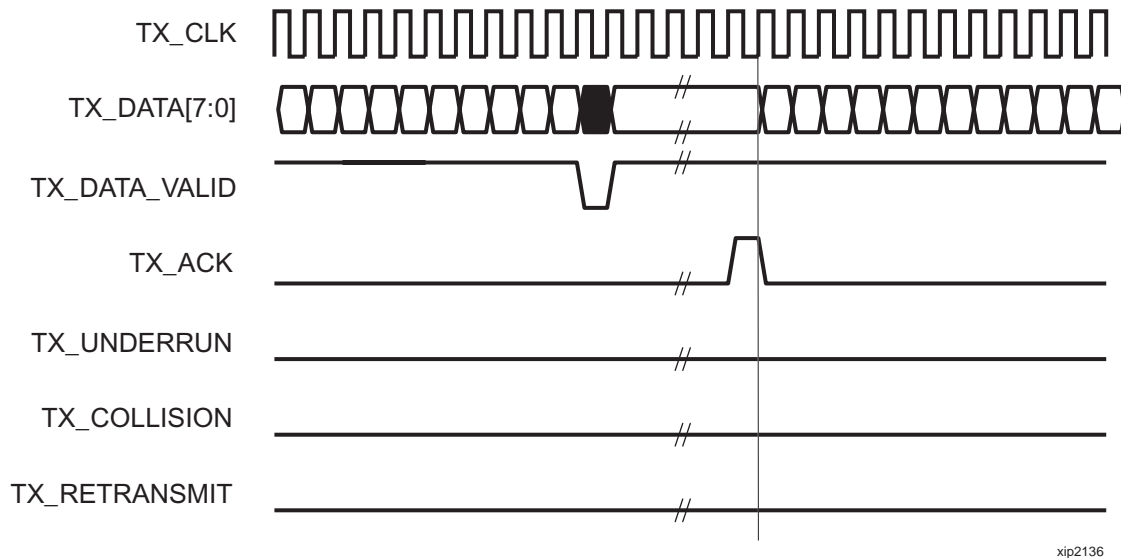
Figure 11: Frame Transmission with Underrun

Back-to-Back Transfers

Figure 12 shows the case where the MAC client is immediately ready to transmit a second frame of data following completion of its first frame. In this figure, the end of the first frame is shown on the left. On the clock cycle immediately following the final byte of the first frame, TX_DATA_VALID is taken low by the client, and is taken high one clock cycle later to indicate that the first byte of the destination address of the second frame is on TX_DATA awaiting transmission.

When the MAC core is ready to accept data, TX_ACK is asserted and the transmission continues in the same manner as in the case of the single frame. The MAC core will defer the assertion of TX_ACK appropriately to comply with inter-packet gap requirements and flow control requests.

If the MAC core is operating in half-duplex mode, the timing shown in Figure 12 is required to take advantage of frame bursting; the MAC core is only guaranteed to retain control of the medium if the TX_DATA_VALID signal is low for a single clock cycle. For more information on frame bursting, see IEEE 802.3-2002.



xip2136

Figure 12: Back to Back Frame Transmission

VLAN Tagged Frames

Transmission of a VLAN tagged frame (if enabled) can be seen in [Figure 13](#). Note that the handshaking signals across the interface do not change; however, the VLAN type tag 81-00 must be supplied by the client to signify that

the frame is VLAN tagged. The client also supplies the two bytes of Tag Control Information, V1 and V2, at the appropriate times in the data stream. More information on the contents of these two bytes can be found in IEEE 802.3-2002.

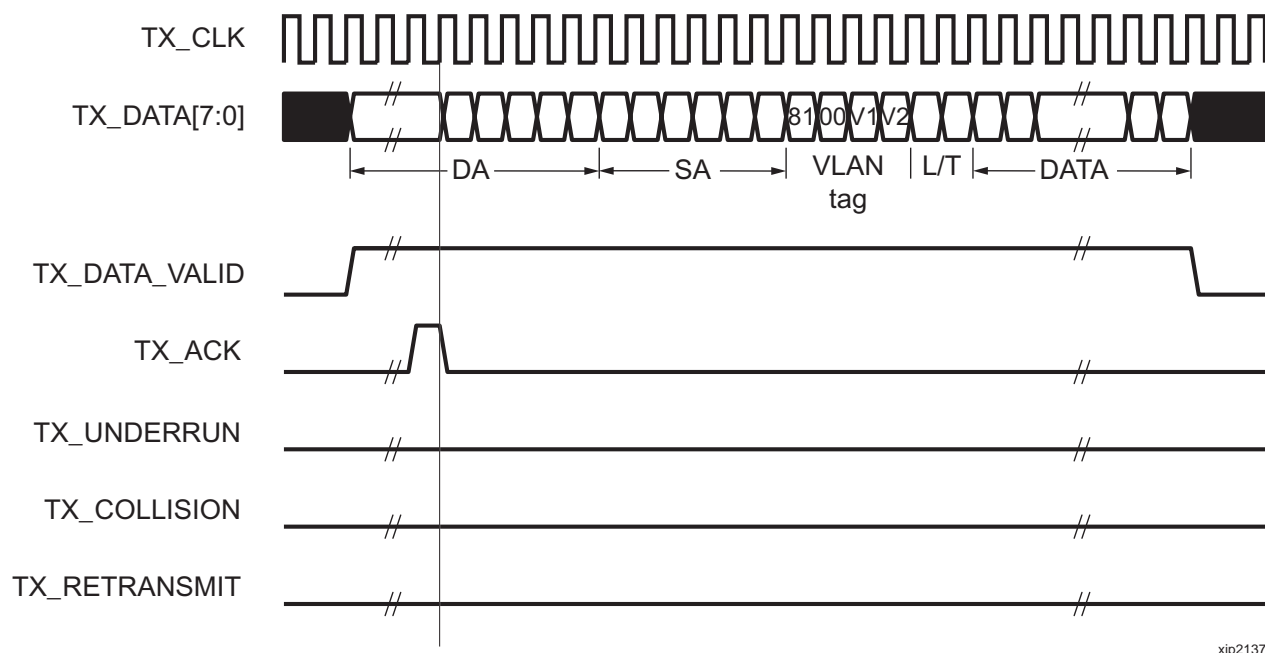


Figure 13: Transmission of a VLAN Tagged Frame

Maximum Permitted Frame Length

The maximum legal length of a frame specified in IEEE 802.3-2002 is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames may be extended to 1522 bytes. When jumbo frame handling is disabled and the client attempts to transmit a frame which exceeds the maximum legal length, the MAC core will insert an error code to cor-

rupt the current frame and the frame will be truncated to the maximum legal length. When jumbo frame handling is enabled, frames which are longer than the legal maximum are transmitted error-free.

For more information on enabling and disabling jumbo frame handling, see ["Configuration Registers" on page 30](#).

Frame Collisions - Half Duplex Operation Only

In half duplex Ethernet operation, collisions will occur on the medium as a matter of course; this is how the arbitration algorithm is fulfilled. In case of a collision, the MAC core signals to the client that data may need to be resupplied as follows.

If there is a collision, the TX_COLLISION signal will be set to "1" by the MAC core. If a frame is in progress, the client must abort the transfer and take TX_DATA_VALID to "0."

If the TX_RETRANSMIT signal is "1" in the same clock cycle that the TX_COLLISION signal is "1," the client must

resubmit the previous frame to the MAC core for retransmission; TX_DATA_VALID must be asserted to the MAC core within 8 clock cycles of the TX_COLLISION signal in order to meet Ethernet timing requirements. See Figure 14.

If the TX_RETRANSMIT signal is "0" in the same clock cycle that the TX_COLLISION signal is "1," the number of retries for this frame has exceeded the Ethernet specification and the frame should be dropped by the client. The client can then make any new frame available to the MAC for transmission without timing restriction. See Figure 15.

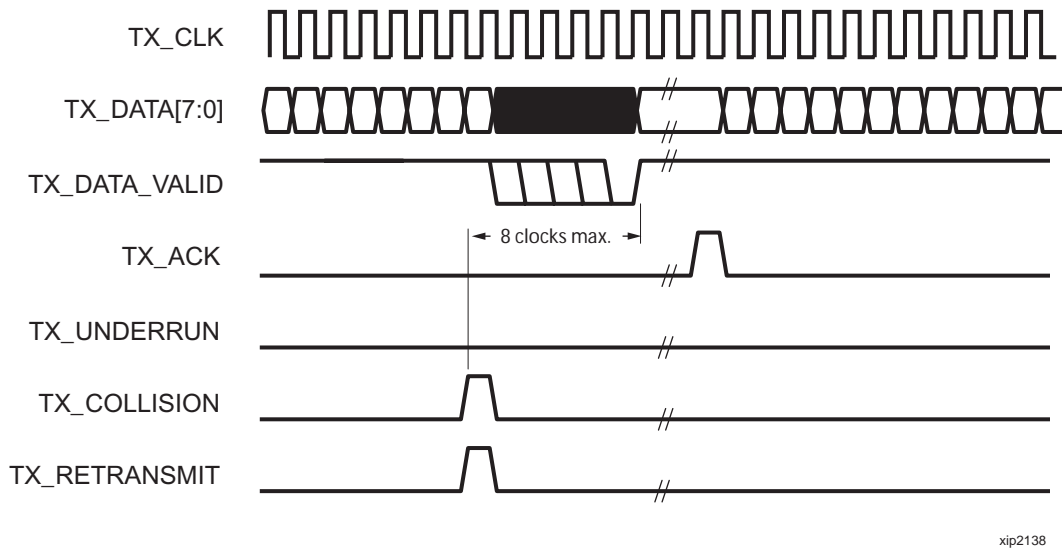


Figure 14: Collision Handling - Frame retransmission required

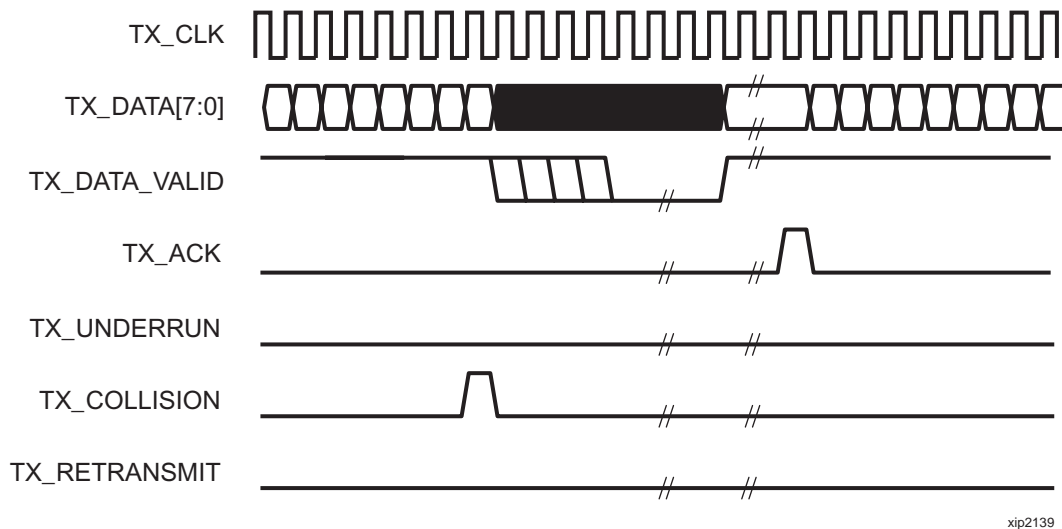


Figure 15: Collision Handling - No frame retransmission required

Interframe Gap Adjustment

The user can elect to vary the length of the inter frame gap. If this function is selected (via a configuration bit in the transmitter control register, see "Configuration Registers" on page 30) then the MAC will exert back pressure to delay the transmission of the next frame until the requested number of Idle cycles has elapsed. The number of Idle cycles is controlled by the value on the TX_IFG_DELAY port at the start of frame transmission; Figure 16 shows the MAC operating in this mode.

Reducing the Inter frame gap to below the IEEE 802.3-2002 minimum of 12 Idles is supported in Full Duplex only designs and will transmit an absolute minimum of 4 Idles. If the Interframe gap adjustment is reduced below 12 Idles, then the accuracy of the Optional Statistical Gathering (*statistics_gathering=true*) Counters cannot be guaranteed. However, the TX_STATISTIC_VECTOR and RX_STATISTIC_VECTOR will always remain correct.

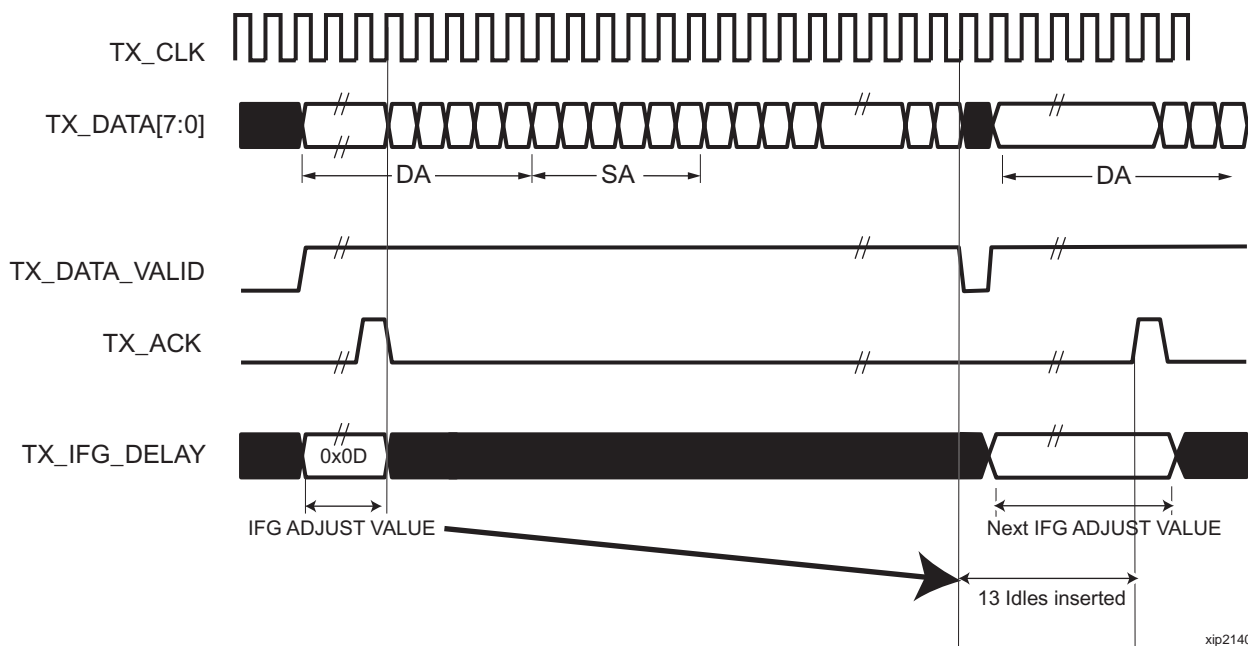


Figure 16: Interframe Gap Adjustment

Transmitter Statistics Vector

The statistics for the frame transmitted are contained within the TX_STATISTICS_VECTOR. The vector is driven synchronously by the transmitter clock, TX_CLK, following frame transmission. The bit field definition for the Vector is defined in Table 14.

All bit fields, with the exception of BYTE_VALID are valid only when the TX_STATISTICS_VALID is asserted. This is illustrated in Figure 17. BYTE_VALID is significant on every TX_CLK cycle.

TX_STATISTICS_VECTOR bits 25 down to 17 inclusive are for half duplex only and will be set to logic 0 when operating in full duplex mode.

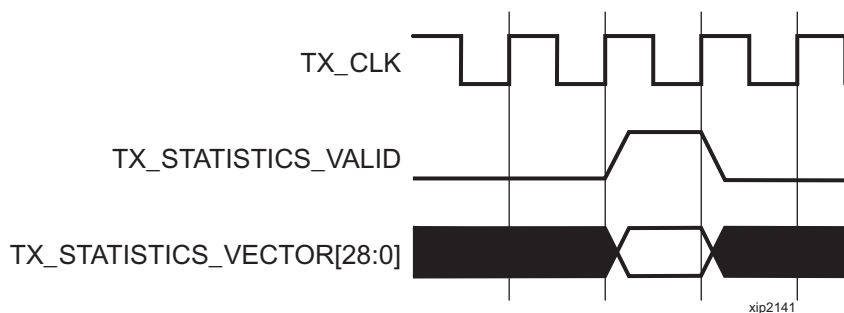


Figure 17: Transmitter Statistics Vector Timing

Table 14: Bit Definition for the Transmitter Statistics Vector

TX_STATISTICS_VECTOR	Name	Description
28	PAUSE_FRAME_TRANSMITTED	Asserted if the previous frame was a pause frame that the MAC itself initiated in response to a PAUSE_REQ assertion.
27	BYTE_VALID	Asserted if a MAC frame byte (DA to FCS inclusive) is in the process of being transmitted. This is valid on every clock cycle. Do not use this as an enable signal to indicate that data is present on GMII_TXD[7:0].
26	Reserved	Returns logic 0.
25 down to 22	TX_ATTEMPTS[3:0]	The number of attempts that have been made to transmit the previous frame. This is a 4-bit number: 0 should be interpreted as 1 attempt; 1 as 2 attempts, up until 15 as 16 attempts.
21	Reserved	Returns logic 0.
20	EXCESSIVE_COLLISION	Asserted if a collision has been detected on each of the last 16 attempts to transmit the previous frame.
19	LATE_COLLISION	Asserted if a late collision occurred during frame transmission.
18	EXCESSIVE_DEFERRAL	Asserted if the previous frame was deferred for an excessive amount of time as defined by the constant "maxDeferTime" in IEEE 802.3-2002.
17	TX_DEFERRED	Asserted if transmission of the frame was deferred.
16	VLAN_FRAME	Asserted if the previous frame contained a VLAN identifier in the Length/Type field when transmitter VLAN operation is enabled.
15 down to 5	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count will stick at 2047 for any Jumbo frames larger than this value.
4	CONTROL_FRAME	Asserted if the previous frame had the special MAC Control Type code 88-08 in the Length/Type field.
3	UNDERRUN_FRAME	Asserted if the previous frame contained an underrun error.
2	MULTICAST_FRAME	Asserted if the previous frame contained a multicast address in the Destination Address field.
1	BROADCAST_FRAME	Asserted if the previous frame contained a broadcast address in the Destination Address field.
0	SUCCESSFUL_FRAME	Asserted if the previous frame was transmitted without error.

Receiver

Normal Frame Reception

The timing of a normal inbound frame transfer can be seen in [Figure 18](#). The client must be prepared to accept data at any time; there is no buffering within the MAC to allow for latency in the receive client. Once frame reception begins,

data is transferred on consecutive clock cycles to the receive client until the frame is complete. The MAC asserts the `RX_GOOD_FRAME` signal to indicate that the frame was successfully received and that the frame should be analyzed by the client.

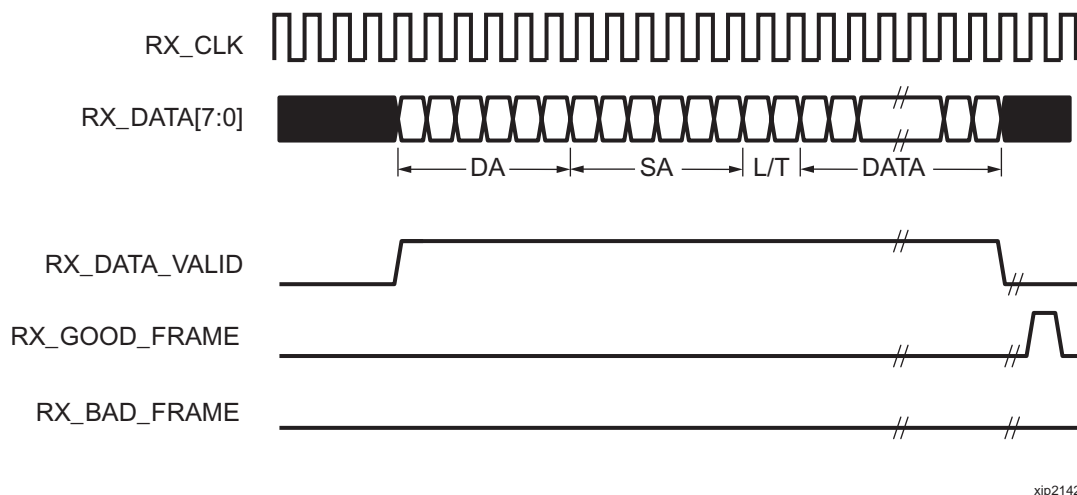


Figure 18: Normal Frame Reception

Frame parameters (destination address, source address, length/type and optionally FCS) are supplied on the data bus according to the timing diagram. The abbreviations are the same as those described in [Table 13 on page 16](#).

If the Length/Type field in the frame has the Length interpretation, and this indicates that the inbound frame has been padded to meet the Ethernet minimum frame size specification, then this padding will not be passed to the client in the data payload. The exception to this is in the case where FCS passing is enabled, see ["Client-Supplied FCS Passing" on page 25](#).

Therefore, when Client-Supplied FCS passing is disabled, `RX_DATA_VALID` = '0' between frames for the duration of the Padding field (if present), the FCS field, carrier extension (if present), the interframe gap following the frame, and the preamble field of the next frame. When Client-Supplied

FCS passing is enabled, `RX_DATA_VALID` = '0' between frames for the duration of carrier extension (if present), the interframe gap, and the preamble field of the following frame.

RX_GOOD_FRAME, RX_BAD_FRAME timing

Although the timing diagram in [Figure 18](#) shows the `RX_GOOD_FRAME` signal asserted shortly after the last valid data on `RX_DATA`, this is not always the case. The `RX_GOOD_FRAME` or `RX_BAD_FRAME` signals are asserted only after all frame checks are completed. This is after the FCS field has been received (and after reception of carrier extension, if present).

Therefore, either `RX_GOOD_FRAME` or `RX_BAD_FRAME` is asserted following frame reception at the beginning of the interframe gap.

Frame Reception with Errors

The case of an unsuccessful frame reception (for example, a fragment frame or a frame with an incorrect FCS) can be seen in Figure 19. In this case, the RX_BAD_FRAME signal

is asserted to the client at the end of the frame. It is then the responsibility of the client to drop the data already transferred for this frame.

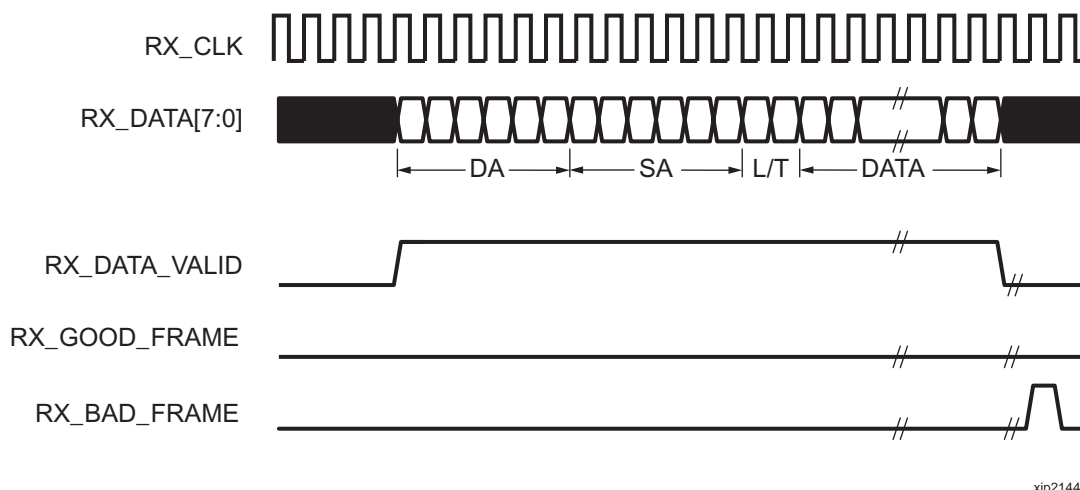


Figure 19: Frame Reception with Error

Client-Supplied FCS Passing

If the MAC core is configured to pass the FCS field to the client (see "Configuration Registers" on page 30), then this is handled as shown in Figure 20.

In this case, any padding inserted into the frame to meet Ethernet minimum frame length specifications will be left intact and passed to the client.

Note that even though the FCS is passed up to the client, it is also verified by the MAC core, and RX_BAD_FRAME asserted if the FCS check fails.

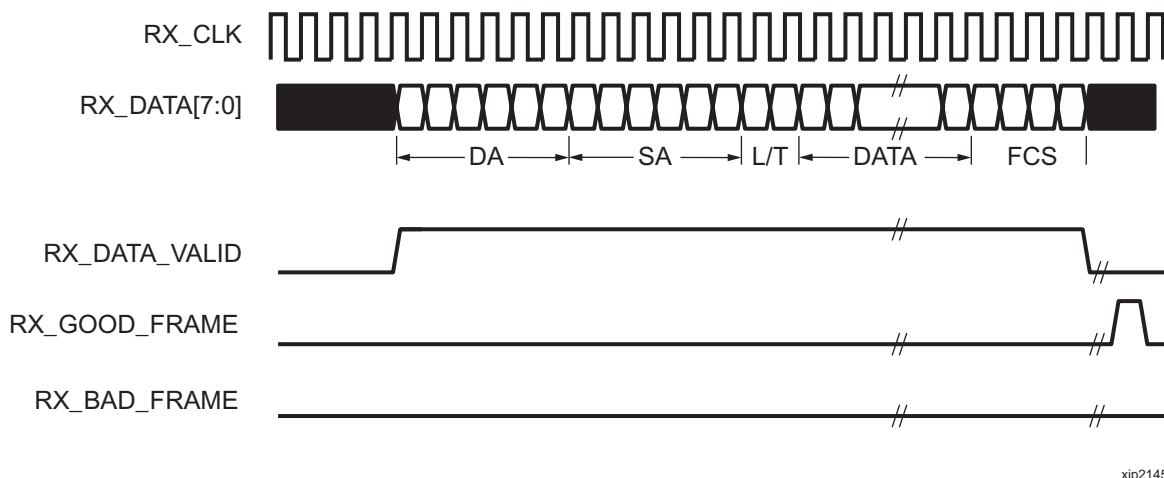


Figure 20: Frame Reception with In-Band FCS Field

VLAN Tagged Frames

The reception of a VLAN tagged frame (if enabled) can be seen in [Figure 21](#). The VLAN frame is passed to the client so that the frame may be identified as VLAN tagged; this is

followed by the Tag Control Information bytes, V1 and V2. More information on the interpretation of these bytes may be found in IEEE 802.3-2002 standard.

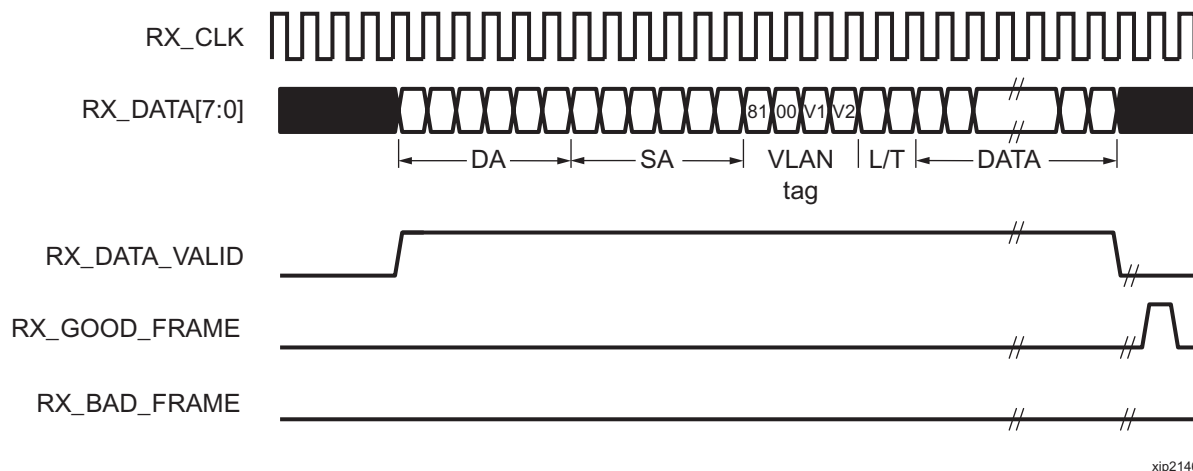


Figure 21: Reception of a VLAN Tagged Frame

Maximum Permitted Frame Length

The maximum legal length of a frame specified in IEEE 802.3-2002 is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames may be extended to 1522 bytes. When jumbo frame handling is disabled and the core receives a frame which exceeds the maximum legal length, RX_BAD_FRAME will be asserted. When jumbo frame handling is enabled, frames which are longer than the legal maximum are received in the same way as shorter frames.

For more information on enabling and disabling jumbo frame handling, see ["Configuration Registers" on page 30](#).

Length/Type Field Error Checks

Enabled

Default operation is with the Length/Type error checking enabled (see ["Receiver Configuration Word 1" on page 31](#)). In this mode the following checks are made on all frames received. If either of these checks fail then the frame is marked as BAD.

- A value in the Length/Type field that is greater than or equal to decimal 46 but less than decimal 1536 (a Length interpretation) is checked against the actual data length received.

- A value in the Length/Type field that is less than decimal 46 is checked to see that the data field is padded to exactly 46 bytes (so that the resultant frame is minimum frame size: 64 bytes total in length).

Furthermore, if Padding is indicated (the Length/Type field is less than decimal 46) and [Client-Supplied FCS Passing](#) is disabled, then the Length value in the Length/Type field will be used to deassert RX_DATA_VALID after the indicated number of data bytes so that the Padding bytes are removed from the frame.

Disabled

When the Length/Type error checking is disabled (see ["Receiver Configuration Word 1" on page 31](#)) the Length/Type error checks described above are not performed. A frame containing only these errors will be marked as GOOD.

Furthermore, if Padding is indicated and [Client-Supplied FCS Passing](#) is disabled, then a Length Value in the Length/Type field will not be used to deassert RX_DATA_VALID. Instead RX_DATA_VALID will be deasserted before the start of the FCS field; in this way any padding will not be removed from the frame.

Receiver Statistics Vector

The statistics for the frame received are contained within the RX_STATISTICS_VECTOR. The vector is driven synchronously by the receiver clock, RX_CLK following frame reception. The bit field definition for the Vector is defined in [Table 15](#).

All bit fields, with the exception of BYTE_VALID are valid only when the RX_STATISTICS_VALID is asserted. This is illustrated in [Figure 22](#). BYTE_VALID is significant on every RX_CLK cycle.

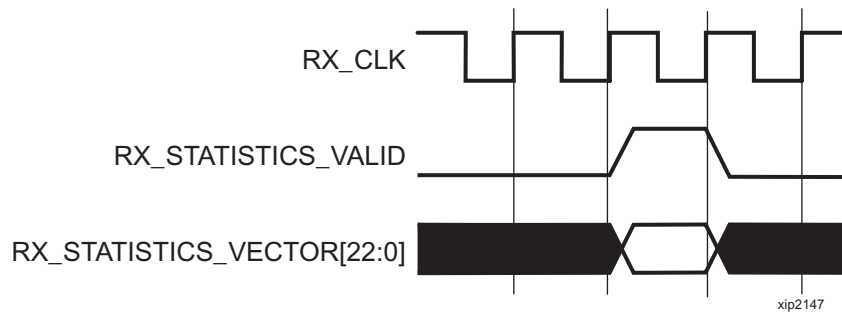


Figure 22: Receiver Statistics Vector Timing

Table 15: Bit Definition for the Receiver Statistics Vector

RX_STATISTICS_VECTOR	Name	Description
22	LENGTH/TYPE Out of Range	Asserted if the length/type field contained a length value that did not match the number of MAC client data bytes received. Also high if the length/type field indicated that the frame contained padding but the number of MAC client data bytes received was not equal to 64 bytes (minimum frame size). The exception to the above is when the Length/Type Field Error Checks are disabled, in which case this bit will not be asserted.
21	BAD_OPCODE	Asserted if the previous frame was error-free and contained the special Control Frame identifier in the Length/Type field, but contained an opcode that is unsupported by the MAC (Any Opcode other than PAUSE).
20	FLOW_CONTROL_FRAME	Asserted if the previous frame was error-free, contained the special Control Frame identifier in the Length/Type field, contained a Destination Address that matched either the MAC Control Multicast Address or the configured source address of the MAC, contained the supported PAUSE opcode, and was acted upon by the MAC.
19	BYTE_VALID	Asserted if a MAC frame byte (DA to FCS inclusive) is in the process of being received. This is valid on every clock cycle. Do not use this as an enable signal to indicate that data is present on RX_DATA[7:0].
18	VLAN_FRAME	Asserted if the previous frame contained a VLAN identifier in the Length/Type field when receiver VLAN operation is enabled.

Table 15: Bit Definition for the Receiver Statistics Vector

RX_STATISTICS_VECTOR	Name	Description
17	OUT_OF_BOUNDS	Asserted if the previous frame exceeded the specified IEEE802.3-2002 maximum legal length (see "Maximum Permitted Frame Length" on page 26). This is only valid if Jumbo frames are disabled.
16	CONTROL_FRAME	Asserted if the previous frame contained the special Control Frame identifier in the Length/Type field.
15 down to 5	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count will stick at 2047 for any Jumbo frames larger than this value.
4	MULTICAST_FRAME	Asserted if the previous frame contained a multicast address in the Destination Address field.
3	BROADCAST_FRAME	Asserted if the previous frame contained the broadcast address in the Destination Address field.
2	FCS_ERROR	Asserted if the previous frame received had an incorrect FCS value or the MAC detected error codes during frame reception.
1	BAD_FRAME ¹	Asserted if the previous frame received contained errors.
0	GOOD_FRAME ¹	Asserted if the previous frame received was error-free.

1. If the **Length/Type Field Error Checks** are disabled then a frame which contains this type of error will be marked as a GOOD_FRAME providing no additional errors were detected.

Flow Control

The flow control block is designed to Clause 31 of the IEEE 802.3-2002 standard. The MAC may be configured to send pause frames and to act upon their reception. These two behaviors can be configured asymmetrically; see ["Configuration Registers" on page 30](#).

Transmitting a PAUSE Control Frame

The client initiates a flow control frame by asserting PAUSE_REQ while the pause value is on the PAUSE_VAL bus. These signals are synchronous to TX_CLK. The timing of this can be seen in [Figure 23](#).

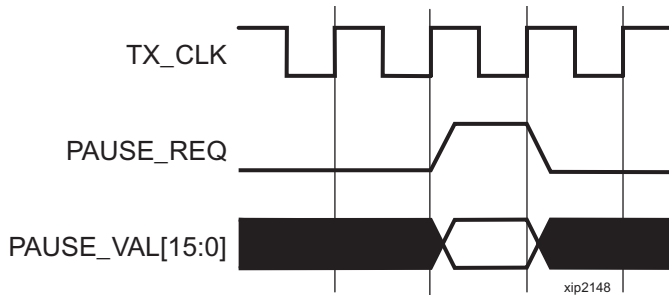


Figure 23: Pause Request Timing

If the MAC core is configured to support transmit flow control, this action causes the core to transmit a PAUSE control frame on the link, with the PAUSE parameter set to the value on PAUSE_VAL in the cycle when PAUSE_REQ was asserted. This will not disrupt any frame transmission in progress but will take priority over any pending frame trans-

mission. This frame will be transmitted even if the transmitter is in the paused state itself.

Receiving a Pause Control Frame

When an error-free frame is received by the MAC core, the following checks are made:

1. The Destination Address field is matched against the MAC Control Multicast address or the configured Source Address for the MAC (see ["Configuration Registers" on page 30](#)).
2. The Length/Type field is matched against the MAC Control Type code.
3. The opcode field contents are matched against the PAUSE opcode if check 2 is true.

If any of the above checks are false or the MAC Flow Control logic for the receiver is disabled, the frame is ignored by the Flow Control logic and passed up to the client.

If the frame passes all of the above checks, is of minimum legal size and the MAC Flow Control logic for the receiver is enabled, the pause value parameter in the frame is then used to inhibit transmitter operation for the time defined in the IEEE802.3-2002 specification. This inhibit is implemented using the same back pressure scheme shown in [Figure 12](#). Because the received pause frame has been acted upon, it is passed to the client with RX_BAD_FRAME asserted to indicate to the client that it should be dropped.

Reception of any frame for which check 2 is true and which is not of legal minimum length is considered an invalid Control frame. This will be ignored by the Flow Control logic and passed to the client with RX_BAD_FRAME asserted.

Optional Management Interface (management_interface=true)

The management interface is a processor-independent interface with standard address, data and control signals. It may be used as is, or a wrapper may be applied (not supplied) to interface to common bus architectures.

This interface is used for:

- Configuration of the MAC core;
- Access to optional statistics counters for use by higher layers, for example, SNMP
- access through the MDIO interface to the management registers located in the PHY attached to the MAC core.

The management interface is accessed differently depending on the type of transaction; a truth table showing which access method is required for each transaction type is shown in [Table 16](#). These access methods are described in the following sections.

Table 16: Management Interface Transaction Types

Transaction	HOST_MIIM_SEL	HOST_ADDR[9]
Configuration	0	1
Statistics	0	0
MIIM access	1	X

Table 17: Configuration Registers

Address	Description
0x200-0x23F	Receiver Configuration (Word 0).
0x240-0x27F	Receiver Configuration (Word 1).
0x280-0x2BF	Transmitter Configuration.
0x2C0-0x2FF	Flow Control Configuration.
0x300-0x33F	Reserved.
0x340-0x37F	Management Configuration.

HOST_CLK Frequency

The management interface clock, HOST_CLK, is used to derive the MDIO clock, MDC, and is therefore subject to some frequency restrictions. This HOST_CLK must be:

≥ 10 MHz

≤ 100 MHz

Configuring the MAC core to derive the MDC signal from this clock is detailed in ["MDIO Interface" on page 37](#).

Configuration Registers

After power up or reset, the client may reconfigure the core parameters from their defaults, such as flow control support. Configuration changes can be written at any time. Both the receiver and transmitter logic will only respond to configuration changes during Inter Frame Gaps. The exceptions to this are the configurable resets which take effect immediately.

Configuration of the MAC core is performed through a register bank accessed through the management interface. The configuration registers available in the core are detailed in [Table 17](#). As can be seen, the address has some implicit don't care bits; any access to an address in the ranges shown will perform a 32-bit read or write from the same configuration word.

The register contents for the two receiver configuration words can be seen in [Table 18](#) and [Table 19](#).

Table 18: Receiver Configuration Word 0

Bit	Default Value	Description
31-0	All 0's	<p>Pause frame MAC Source Address[31:0]. This address is used by the MAC to match against the Destination Address of any incoming flow control frames. It is also used by the flow control block as the Source Address (SA) for any outbound flow control frames.</p> <p>The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Address[47:0] as 0xFFEEDDCCBBAA.</p>

Table 19: Receiver Configuration Word 1

Bit	Default Value	Description
15-0	All 0's	Pause frame MAC Source Address[47:32]. See description in Table 18 .
24-16	N/A	Reserved.
25	0	Length/Type Error Check Disable. When this bit is set to "1", the core will not perform the Length/Type field error checks as described in " Length/Type Field Error Checks " on page 26. When this bit is set to "0" the Length/Type field checks will be performed: this is normal operation.
26	0	Half Duplex. If "1," the receiver will operate in half duplex mode. If "0," the receiver will operate in full duplex mode. Has no effect if XCO parameter half_duplex_capable = false.
27	0	VLAN Enable. When this bit is set to "1," VLAN tagged frames will be accepted by the receiver.
28	1	Receiver Enable. If set to "1," the receiver block will be operational. If set to "0," the block will ignore activity on the physical interface RX port.
29	0	In-band FCS Enable. When this bit is "1," the MAC receiver will pass the FCS field up to the client as described in " Client-Supplied FCS Passing " on page 25. When it is "0," the client will not be passed the FCS. In both cases, the FCS will be verified on the frame.
30	0	Jumbo Frame Enable. When this bit is set to "1," the MAC receiver will accept frames over the specified IEEE802.3-2002 maximum legal length. When this bit is "0," the MAC will only accept frames up to the specified maximum.
31	0	Reset. When this bit is set to "1," the receiver will be reset. The bit will then automatically revert to "0." Note that this reset will also set all of the receiver configuration registers to their default values.

Notes:

1. In changing the receiver's mode from Half Duplex to Full Duplex, there is a period of time of up to 2.4 us following the mode change when no new receiver statistics can be stored in the optional Statistical Counters.

The register contents for the Transmitter Configuration Word are described in [Table 20](#).

Table 20: Transmitter Configuration Word

Bit	Default Value	Description
24-0	N/A	Reserved
25	0	Interframe Gap Adjust Enable. If '1', the transmitter will read the value on the port TX_IFG_DELAY at the start of frame transmission and adjust the interframe gap following the frame accordingly. See "Interframe Gap Adjustment" on page 22 . If "0," the transmitter will output a minimum Inter Frame Gap of twelve clock cycles, as specified in IEEE802.3-2002.
26	0	Half Duplex. If '1', the transmitter will operate in half duplex mode. If '0', the transmitter will operate in full duplex mode. Has no effect if XCO parameter half_duplex_capable = false.
27	0	VLAN Enable. When this bit is set to 1, the transmitter will allow the transmission of VLAN tagged frames.
28	1	Transmit Enable. When this bit is 1, the transmitter is operational. When it is 0, the transmitter is disabled.
29	0	In-band FCS Enable. When this bit is '1', the MAC transmitter will expect the FCS field to be passed in by the client as described in "Client-Supplied FCS Passing" on page 17 . When this bit is "0," the MAC transmitter will append padding as required, compute the FCS and append it to the frame.
30	0	Jumbo Frame Enable. When this bit is set to "1," the MAC transmitter will send frames that are greater than the specified IEEE802.3-2002 maximum legal length. When this bit is "0," the MAC will only send frames up to the specified maximum.
31	0	Reset. When this bit is set to "1," the transmitter will be reset. The bit will then automatically revert to "0." Note that this reset will also set all of the transmitter configuration registers to their default values.

Notes:

1. In changing the transmitter's mode from Half Duplex to Full Duplex, there is a period of time of up to 2.4 us following the mode change when no new transmitter statistics can be stored in the optional Statistical Counters.

The register contents for the Flow Control Configuration Word are described in [Table 21](#).

Table 21: Flow Control Configuration Word

Bit	Default Value	Description
28-0	N/A	Reserved
29	1	Flow Control Enable (RX). When this bit is '1', received flow control frames will inhibit the transmitter operation as described in "Receiving a Pause Control Frame" on page 29 . When this bit is '0', received flow control frames will always be passed up to the client.
30	1	Flow Control Enable (TX). When this bit is '1', asserting the PAUSE_REQ signal will send a flow control frame out from the transmitter. When this bit is 0, asserting the PAUSE_REQ signal has no effect.
31	N/A	Reserved

The register contents for the Management Configuration Word are described in [Table 22](#).

Table 22: Management Configuration Word

Bits	Default Value	Description
4-0	All 0's	Clock Divide[4:0]. See "MDIO Interface" on page 37 .
5	0	MDIO Enable. When this bit is 1, the MDIO interface can be used to access attached PHY devices. When this bit is 0, the MDIO interface is disabled and the MDIO signals remain inactive.
31-6	N/A	Reserved

Writing to the configuration registers through the management interface is depicted in [Figure 24](#). When accessing the configuration registers (i.e. when `HOST_ADDR[9] = '1'` and `HOST_MIIM_SEL = '0'`), the upper bit of `HOST_OPCODE` functions as an Active Low write enable signal. The lower `HOST_OPCODE` bit is a "don't care."

Reading from the configuration register words is similar, but the upper `HOST_OPCODE` bit should be '1'. This is shown in [Figure 25](#). In this case, the contents of the register appear on `HOST_RD_DATA` the `HOST_CLK` edge after the register address is asserted onto `HOST_ADDR`.

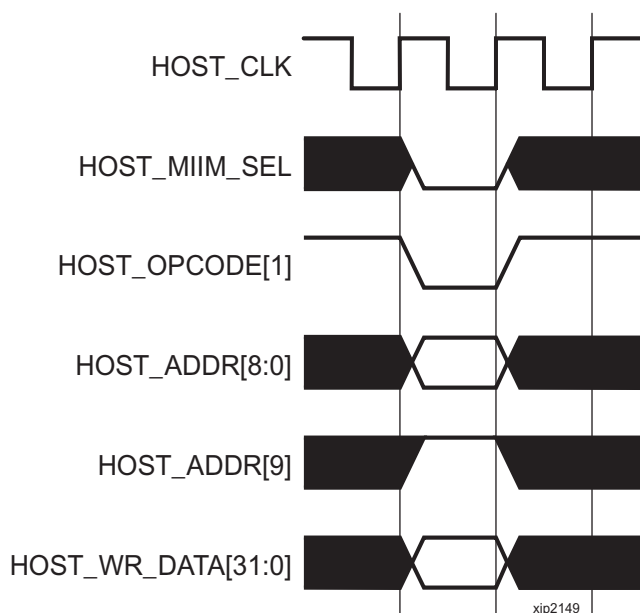


Figure 24: Configuration Register Write Timing

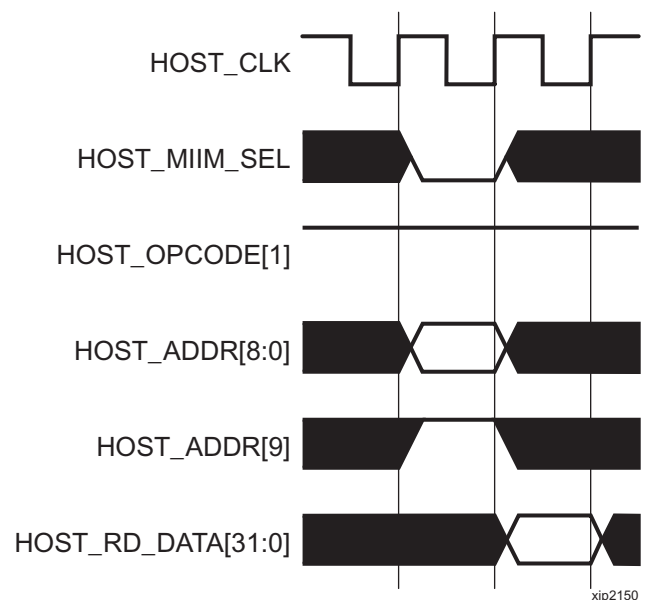


Figure 25: Configuration Register Read Timing

Optional Statistical Gathering (*statistics_gathering=true*)

During operation, the MAC core collects statistics on the success and failure of various operations, for processing by

station management entities (STA) further up the protocol stack. These statistics are accessed by the host through the optional management interface. A complete list of statistics supported is described in [Table 23](#).

Table 23: Statistics Registers

Address	Name	Description
0x000	Frames Received OK. ¹	A count of error-free frames received.
0x001	Frame Check Sequence Errors.	A count of received frames that failed the CRC check and were at least 64 bytes in length.
0x002	Broadcast Frames Received OK. ¹	A count of frames that were successfully received and were directed to the broadcast group address.
0x003	Multicast Frames Received OK. ¹	A count of frames that were successfully received and were directed to a non broadcast group address.
0x004	64 byte Frames Received OK. ¹	A count of error-free frames received that were 64 bytes in length.
0x005	65-127 byte Frames Received OK. ¹	A count of error-free frames received that were between 65 and 127 bytes in length.
0x006	128-255 byte Frames Received OK. ¹	A count of error-free frames received that were between 128 and 255 bytes in length.
0x007	256-511 byte Frames Received OK. ¹	A count of error-free frames received that were between 256 and 511 bytes in length.
0x008	512-1023 byte Frames Received OK. ¹	A count of error-free frames received that were between 512 and 1023 bytes in length.
0x009	1024-MaxFrameSize byte Frames Received OK. ¹	A count of error-free frames received that were between 1024 bytes and the specified IEEE802.3-2002 maximum legal length (see " Maximum Permitted Frame Length " on page 26).
0x00A	Control Frames Received OK.	A count of error-free frames received that contained the special Control Frame identifier in the Length/Type field.
0x00B	Length/Type Out of Range.	<p>A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received.</p> <p>The counter also increments for frames in which the length/type field indicated that the frame contained padding but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size).</p> <p>The exception to the above is when the Length/Type Field Error Checks are disabled in which case this counter will not increment.</p>
0x00C	VLAN Tagged Frames Received OK.	A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation
0x00D	Pause Frames Received OK.	A count of error-free frames received that contained the MAC Control type identifier 88-08 in the Length/Type field, contained a Destination address that matched either the MAC Control multicast address or the configured source address of the MAC, contained the PAUSE opcode and were acted upon by the MAC.
0x00E	Control Frames Received with Unsupported Opcode.	A count of error-free frames received that contained the MAC Control type identifier 88-08 in the Length/Type field but were received with an opcode other than the PAUSE opcode.

Table 23: Statistics Registers (Continued)

Address	Name	Description
0x00F	Oversize Frames Received OK. ¹	A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in IEEE 802.3-2002 (see " Maximum Permitted Frame Length " on page 26).
0x010	Undersize frames received.	A count of the number of frames received that were less than 64 bytes in length but were otherwise well formed.
0x011	Fragment frames received.	A count of the number of frames received that were less than 64 bytes in length and had a bad Frame Check Sequence field.
0x012	Received bytes.	A count of bytes of frames that are received (Destination Address to Frame Check Sequence inclusive).
0x013	Transmitted bytes.	A count of bytes of frames that are transmitted (Destination Address to Frame Check Sequence inclusive).
0x020	Frames Transmitted OK.	A count of error-free frames transmitted.
0x021	Broadcast Frames Transmitted OK.	A count of error-free frames that were transmitted to the broadcast address.
0x022	Multicast Frames Transmitted OK.	A count of error-free frames that were transmitted to a group destination address other than broadcast.
0x023	Underrun Errors.	A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission. This will not count frames which are less than 64 bytes in length.
0x024	Control Frames Transmitted OK.	A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the Length/Type field.
0x025	64 byte Frames Transmitted OK.	A count of error-free frames transmitted that were 64 bytes in length.
0x026	65-127 byte Frames Transmitted OK.	A count of error-free frames transmitted that were between 65 and 127 bytes in length.
0x027	128-255 byte Frames Transmitted OK.	A count of error-free frames transmitted that were between 128 and 255 bytes in length.
0x028	256-511 byte Frames Transmitted OK.	A count of error-free frames transmitted that were between 256 and 511 bytes in length.
0x029	512-1023 byte Frames Transmitted OK.	A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
0x02A	1024-MaxFrameSize byte Frames Transmitted OK.	A count of error-free frames transmitted that were between 1024 and the specified IEEE802.3-2002 maximum legal length (see " Maximum Permitted Frame Length " on page 20).
0x02B	VLAN Tagged Frames Transmitted OK.	A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.
0x02C	Pause Frames Transmitted OK.	A count of error-free PAUSE frames generated and transmitted by the core in response to an assertion of PAUSE_REQ.
0x02D	Oversize Frames Transmitted OK.	A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in IEEE 802.3-2002 (see " Maximum Permitted Frame Length " on page 20).
0x02E	Single Collision Frames.	A count of frames that are involved in a single collision but are subsequently transmitted successfully (Half Duplex Mode only).

Table 23: Statistics Registers (Continued)

Address	Name	Description
0x02F	Multiple Collision Frames.	A count of frames that are involved in more than one collision but are subsequently transmitted successfully (Half Duplex Mode only).
0x040	Frames with Deferred Transmissions	A count of frames whose transmission was delayed on its first attempt because the medium was busy (Half Duplex Mode only).
0x041	Late Collisions	A count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice: both as a collision and as a lateCollision (Half Duplex Mode only).
0x042	Frames Aborted due to Excess collisions.	A count of the frames that, due to excessive collisions, are not transmitted successfully (Half Duplex Mode only).
0x043	Carrier Sense Errors.	A count of times that the GMII_CRS signal was not asserted or was disasserted during the transmission of a frame without collision (Half Duplex Mode only).
0x044	Frames with Excess Deferral	A count of frames that deferred transmission for an excessive period of time (Half Duplex Mode only).

1. If the **Length/Type Field Error Checks** are disabled then these counters will still increment for received frames which contain this type of error (providing no additional errors were detected).

Each of these statistic registers is 64 bits wide and therefore must be read in a two-cycle transfer. The timing of this process is shown in **Figure 26**. Six clocks after the read transaction is initiated, the least significant word (LSW) of the statistics counter appears on the HOST_RD_DATA bus,

and a clock cycle later the most significant word (MSW) appears. For accurate statistic values, 64 clock ticks (of TX_CLK for transmit statistics or RX_CLK for receive statistics) must elapse after the last frame is sent or received through the MAC core.

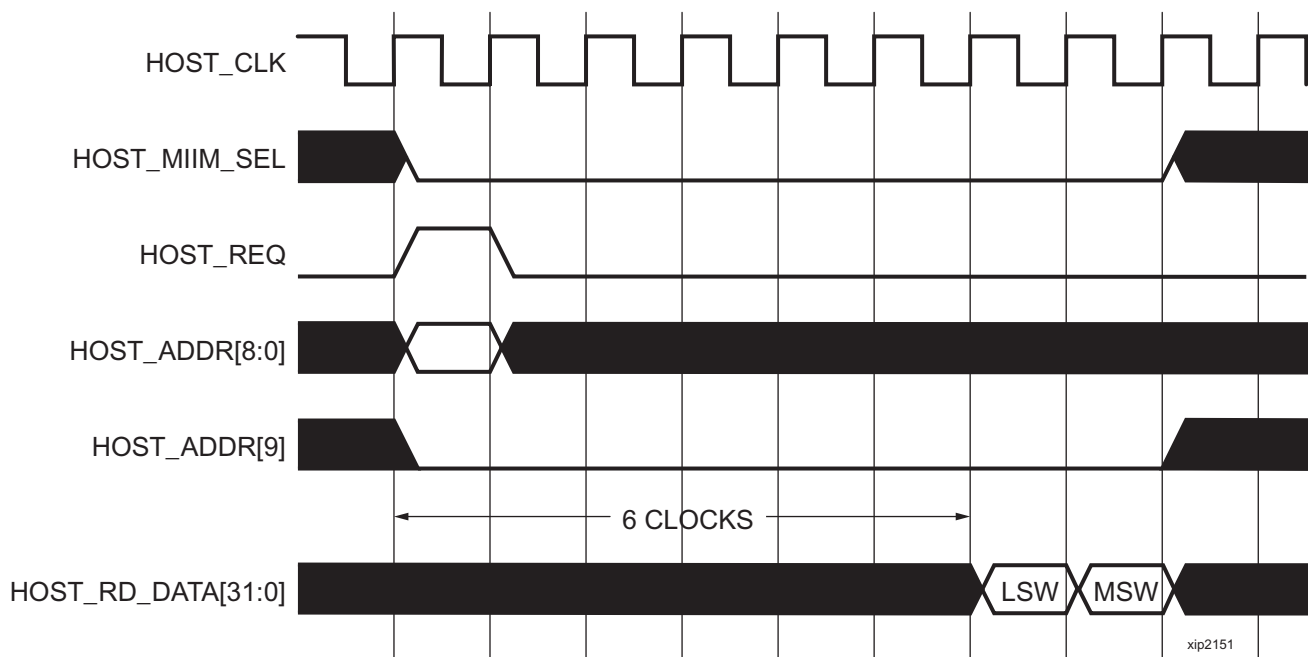


Figure 26: Statistic Register Read Timing

MDIO Interface

The management interface is also used to access the MDIO (MII Management) interface of the MAC core; this interface is used to access the Managed Information Block (MIB) of the PHY components attached to the MAC core.

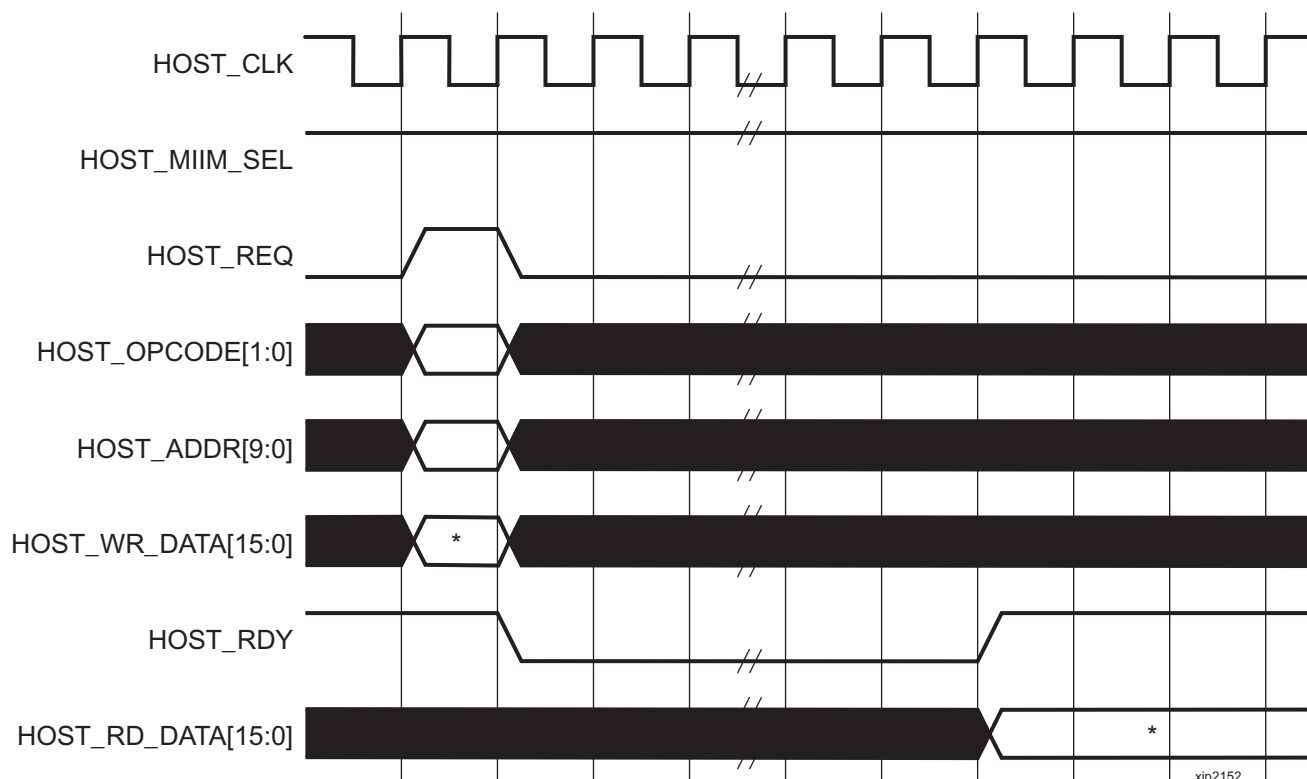
The MDIO interface supplies a clock to the external devices, MDC. This clock is derived from the HOST_CLK signal using the value in the Clock Divide[4:0] configuration register. The frequency of the MDIO clock is given by the following equation:

$$f_{\text{MDC}} = \frac{f_{\text{HOST_CLK}}}{(1 + \text{Clock Divide}[4:0]) \times 2}$$

The frequency of MDC given by this equation should not exceed 2.5 MHz in order to comply with the IEEE 802.3-2002 specification for this interface. To prevent MDC from being out of specification, the Clock Divide[4:0] value powers up at 00000, and while this value is in the register, it is impossible to enable the MDIO interface.

For details of the register map of PHY layer devices and a fuller description of the operation of the MDIO interface itself, see IEEE specification 802.3-2002.

Access to the MDIO interface through the management interface is depicted in the timing diagram in [Figure 27](#).



* If a read transaction is initiated, the HOST_RD_DATA bus is valid at the point indicated. If a write transaction is initiated, the HOST_WR_DATA bus must be valid at the indicated point. Simultaneous read and write is not permitted.

Figure 27: MDIO Access Through Management Interface

For MDIO transactions, the following points apply:

- HOST_OPCODE maps to the OP (opcode) field of the MDIO frame;
- HOST_ADDR maps to the two address fields of the MDIO frame; PHY_ADDR is HOST_ADDR[9:5], and REG_ADDR is HOST_ADDR[4:0].
- HOST_WR_DATA[15:0] maps into the data field of the

MDIO frame when performing a write operation;

- The data field of the MDIO frame maps into HOST_RD_DATA[15:0] when performing a read operation.

The MAC core signals to the host that it is ready for an MDIO transaction by asserting HOST_MIIM_RDY. A read or write transaction on the MDIO is initiated by a pulse on the

HOST_REQ signal. This pulse is ignored if the MDIO interface already has a transaction in progress.

The MAC core then disasserts the HOST_MIIM_RDY signal while the transaction across the MDIO is in progress. When the transaction across the MDIO interface has been completed, the HOST_MIIM_RDY signal will be asserted by the MAC core; if the transaction is a read, the data will also be available on the HOST_RD_DATA[15:0] bus at this time.

Optional Configuration Vector (management_interface = false)

If the optional Management interface is omitted from the core, all of relevant configuration signals are brought out of

the core. These signals are bundled into the CONFIGURATION_VECTOR signal. The bit mapping of the configuration vector signal is defined in [Table 24](#). See the corresponding entry in the configuration register tables for the full description of each signal.

Note that these configuration vector signals can be changed by the user at any time; however, with the exception of the reset and the flow control configuration signals, they will not take effect until the current frame has completed transmission or reception.

The "Clock" heading denotes which clock domain the configuration signal is registered into before use by the core. It is not necessary to drive the signal from this clock domain.

Table 24: Configuration Vector Bit Definition

Bit(s)	Configuration Register cross reference	Clock	Description
47 downto 0	Receiver Configuration Word 0 bits 31-0 and Receiver Configuration Word 1 bits 15-0	RX_CLK	Pause frame MAC Source Address[47:0]. This address is used by the MAC core to match against the Destination Address of any incoming flow control frames, and as the Source Address for any outbound flow control frames. The address is ordered such that the first byte transmitted or received is the least significant byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF will be stored in bite [47:0] as 0xFFEEDDCCBBAA.
48	Receiver Configuration Word 1 bit 26	RX_CLK	Receiver Half Duplex. If '1' the receiver operates in half duplex mode. If '0' the receiver operates in full duplex mode. Has no effect if XCO parameter half_duplex_capable = false.
49	Receiver Configuration Word 1 bit 27	RX_CLK	Receiver VLAN Enable. When this bit is set to '1', VLAN tagged frames are accepted by the receiver.
50	Receiver Configuration Word 1 bit 28	RX_CLK	Receiver Enable. If set to '1', the receiver block is operational. If set to '0', the block ignores activity on the physical interface RX port.
51	Receiver Configuration Word 1 bit 29	RX_CLK	Receiver In-band FCS Enable. When this bit is '1', the MAC receiver will pass the FCS field up to the client as described in "Client-Supplied FCS Passing" on page 25 . When it is '0', the MAC receiver will not pass the FCS field. In both cases, the FCS field will be verified on the frame.
52	Receiver Configuration Word 1 bit 30	RX_CLK	Receiver Jumbo Frame Enable. When this bit is '0', the receiver will not pass frames longer than the maximum legal frame size specified in IEEE 802.3-2002 (see "Maximum Permitted Frame Length" on page 26). When it is '1', the receiver will not have an upper limit on frame size.
53	Receiver Configuration Word 1 bit 31	N/A	Receiver Reset. When this bit is '1', the receiver is held in reset. This signal is an input to the reset circuit for the receiver block. See "Reset circuit" on page 42 for more information.
54	Transmitter Configuration Word bit 25	TX_CLK	Transmitter Interframe Gap Adjust enable. If '1' then the transmitter will read the value of the TX_IFG_DELAY port and set the Interframe Gap accordingly. If '0' the transmitter will always insert at least the legal minimum Interframe Gap.

Table 24: Configuration Vector Bit Definition (Continued)

Bit(s)	Configuration Register cross reference	Clock	Description
55	Transmitter Configuration Word bit 26	TX_CLK	Transmitter Half Duplex. If '1' the transmitter operates in half duplex mode. If '0' the transmitter operates in full duplex mode. Has no effect if XCO parameter half_duplex_capable = false.
56	Transmitter Configuration Word bit 27	TX_CLK	Transmitter VLAN Enable. When this bit is set to '1', the transmitter allows the transmission of VLAN tagged frames.
57	Transmitter Configuration Word bit 28	TX_CLK	Transmitter Enable. When this bit is 1, the transmitter will be operational. When it is 0, the transmitter is disabled.
58	Transmitter Configuration Word bit 29	TX_CLK	Transmitter In-Band FCS Enable. When this bit is '1', the MAC transmitter will expect the FCS field to be pass in by the client as described in "Client-Supplied FCS Passing" on page 17. When it is '0', the MAC transmitter will append padding as required, compute the FCS and append it to the frame.
59	Transmitter Configuration Word bit 30	TX_CLK	Transmitter Jumbo Frame Enable. When this bit is '1', the MAC transmitter will allow frames larger than the maximum legal frame length specified in IEEE 802.3-2002 to be sent. When set to '0', the MAC transmitter will only allow frames up to the legal maximum to be sent.
60	Transmitter Configuration Word bit 31	N/A	Transmitter Reset. When this bit is '1', the MAC transmitter is held in reset. This signal is an input to the reset circuit for the transmitter block. See "Reset circuit" on page 42 for more information.
61	Flow Control Configuration Word bit 29	TX_CLK	Transmit Flow Control Enable. When this bit is '1', asserting the PAUSE_REQ signal causes the MAC core to send a flow control frame out from the transmitter as described in "Receiving a Pause Control Frame" on page 29. When this bit is '0', asserting the PAUSE_REQ signal will have no effect.
62	Flow Control Configuration Word bit 30	RX_CLK	Receive Flow Control Enable. When this bit is '1', received flow control frames will inhibit the transmitter operation as described in "Receiving a Pause Control Frame" on page 29. When it is '0', received flow frames are passed up to the client.
63	Receiver Configuration Word 1 bit 25	RX_CLK	Length/Type Error Check Disable. When this bit is '1', the core will not perform the Length/Type field error checks as described in "Length/Type Field Error Checks" on page 26. When it is set to '0' the Length/Type field checks will be performed: this is normal operation.

Optional GMII (physical_interface=gmi)

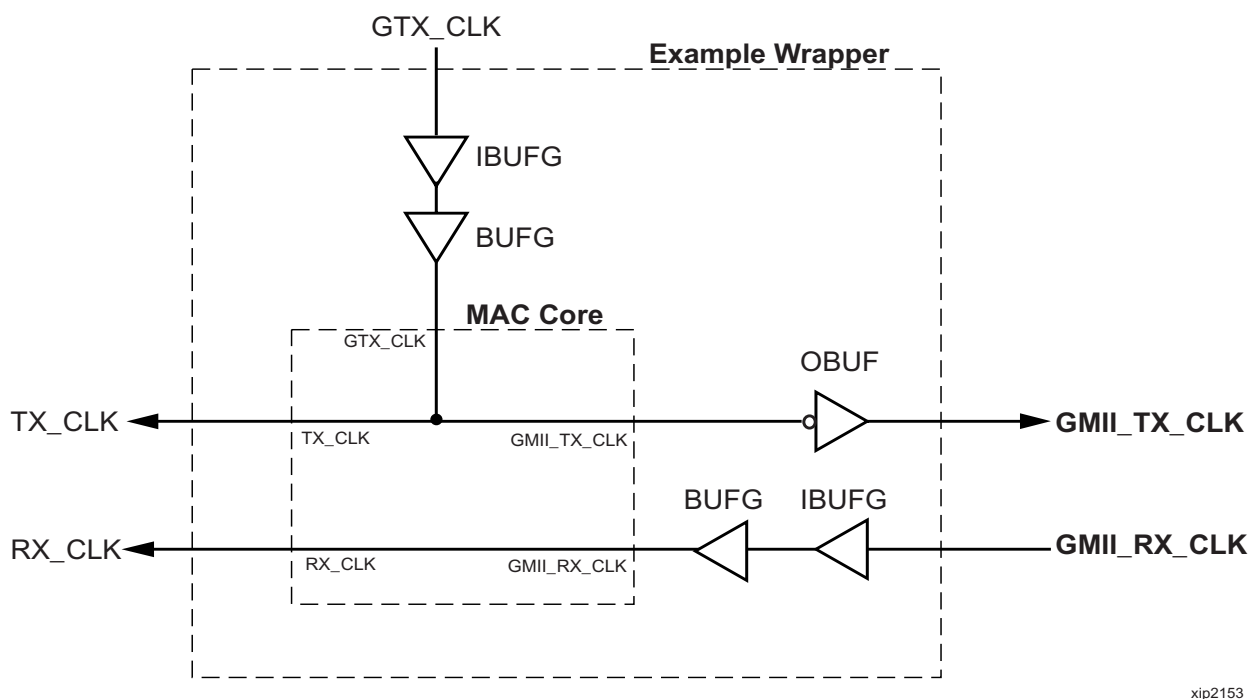
The GMII is designed to IEEE 802.3-2002 Clause 35. This utilizes I/O's of the Xilinx devices, using input/output buffers and input/output flip-flops to maximize setup and hold margins. All I/O logic is placed in the example wrapper that is delivered with the core. In addition, all clock management logic for the core is instantiated in this example wrapper; this allows multiple instances of the core to share clocks. The example wrapper is provided in both VHDL and Verilog.

Clock Management

Figure 28 illustrates the clock management used with the GMII interface. All clocks illustrated have a frequency of 125MHz.

GTX_CLK must be provided to the MAC core. This is a high quality clock which satisfies the IEEE802.3-2002 requirements. It is expected that this clock will be derived from an external oscillator and connected into the device through an IBUFG as illustrated. The clock source must then be routed onto a global clock network by connecting it to a BUFG. Within the MAC core, this global clock is used by all MAC transmitter logic. The MAC Client can obtain this clock by connecting to the TX_CLK signal output from the core. GMII_TX_CLK is derived from this global clock by inverting it and routing it to an OBUF.

GMII_RX_CLK is received through an IBUFG. This clock is then routed onto a global clock network by connecting it to a BUFG. The resulting global clock is used by all MAC receiver logic.



xip2153

Figure 28: Clock Management with GMII

Reset circuit

Internally, the core is divided up into clock/reset domains, which group together elements with the common clock and reset signals. The reset circuitry for one of these domains is illustrated in **Figure 30**. This circuit provides controllable skews on the reset nets within the design.

More information on the operation and rationale behind this circuit can be found in Ken Chapman's Xilinx TechXclusive, "Get Smart About Reset" at <http://www.xilinx.com/support/techxclusives/global-techX19.htm>,

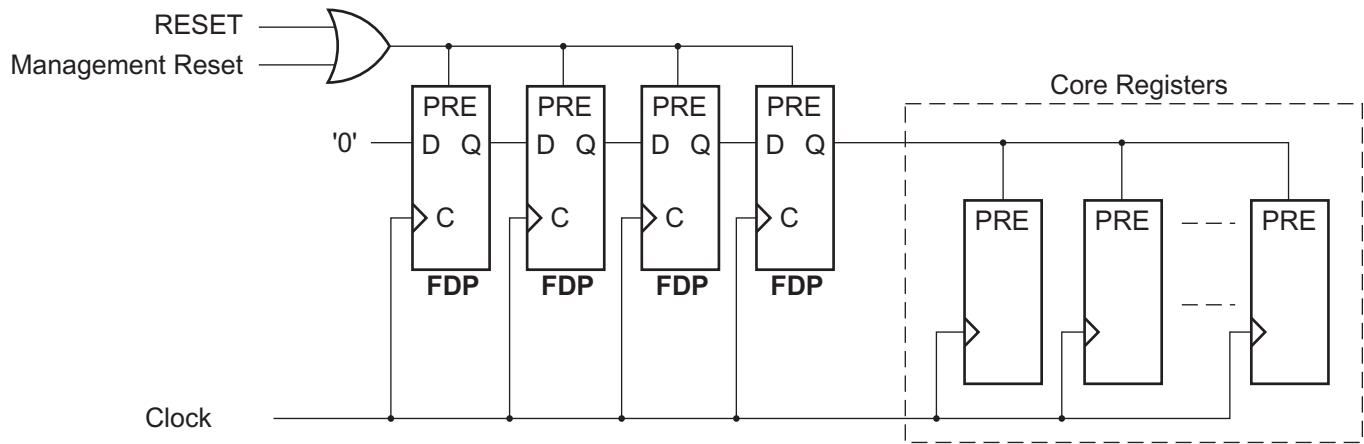


Figure 30: Reset circuit for one clock/reset domain

Optional PCS with Ten-Bit Interface (TBI) for 1000BASE-X (physical_interface=tbi)

The Full-Duplex Physical Coding Sublayer (PCS) for 1000BASE-X is defined in IEEE 802.3-2002 Clauses 36 and 37. This functionality is only available in the Virtex-II and Spartan3 families of FPGA devices.

A block diagram of the PCS is shown in **Figure 31**. The major functional blocks of the PCS are:

- Transmit engine
- Auto-negotiation block
- Receive engine and synchronization block
- PCS managed register block
- 8B/10B encoder block
- 8B/10B decoder block
- Receiver elastic buffer

The PCS Managed Register Block is accessed through the MDIO Interface as if it were an externally connected PHY. This configures the operation of the PCS and Auto-Negotiation. See **"PCS Managed Register Block**

(physical_interface = tbi or phy)" on page 49. The core's optional Management Interface can be used to control the MDIO Interface as described by **"MDIO Interface"** on page 37. When the optional Management Interface is not present, the PCS Managed Register Block must be accessed via an MDIO controller which is not provided by the core.

The 8B/10B encoding/decoding blocks are implemented by configuring two Block SelectRAM modules as ROM. These are used as large look-up tables. The remaining PCS functionality such as code group encoding/decoding, the Managed Register Block, and Auto-Negotiation are implemented in CLB logic.

The Receiver Elastic buffer enables the 10-bit parallel data, received from the PMA sublayer alternatively on PMA_RX_CLK0 and PMA_RX_CLK1 clock edges, to be transferred onto the internal 125MHz clock domain derived from GTX_CLK (see **Clock Management**). This buffer is implemented in Distributed Memory.

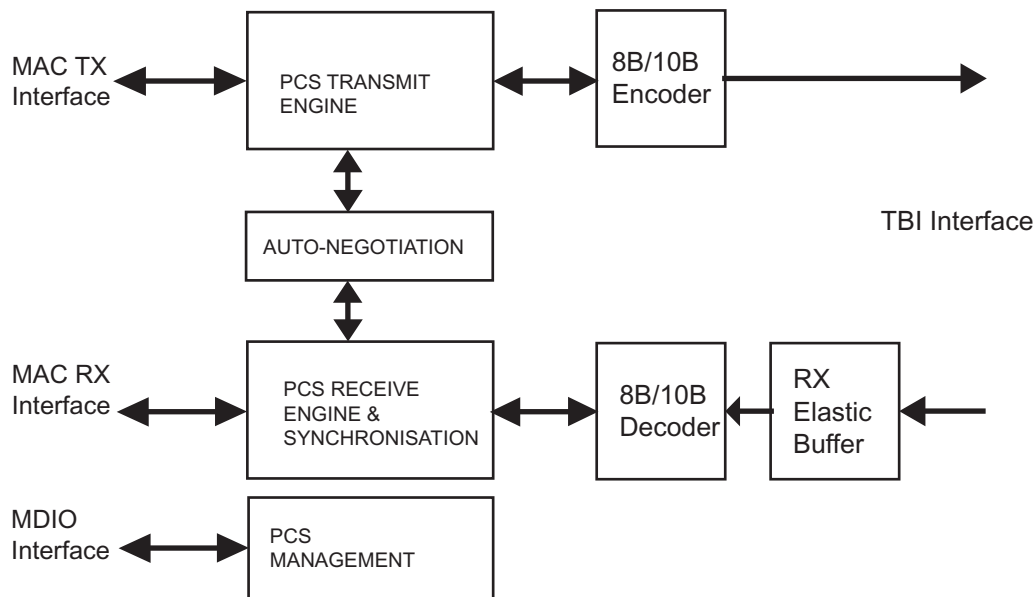


Figure 31: Functional Block Diagram of the 1-Gigabit Ethernet PCS with TBI Interface

TBI Interface

The TBI is designed to IEEE 802.3-2002 Clause 36.3. This utilizes I/O's of the Xilinx devices, using input/output buffers and input/output flip-flops to maximize setup and hold margins. All I/O logic is placed in the example wrapper that is delivered with the core. In addition, all clock management logic for the core is instantiated in this example wrapper; this allows multiple instances of the core to share clocks. The example wrapper is provided in both VHDL and Verilog.

Clock Management

Figure 32 illustrates the clock management used with the TBI interface.

GTX_CLK must be provided to the MAC core. This is a high quality clock of frequency 125MHz which satisfies the IEEE802.3-2002 requirements. It is expected that this clock will be derived from an external oscillator and connected

into the device through an IBUFG as illustrated. The clock source must then be routed onto a global clock network by connecting it to a BUFG. Within the MAC core, this global clock is used by all MAC transmitter logic. PMA_TX_CLK is derived from this global clock by inverting it and routing it to an OBUF.

PMA_RX_CLK0 and PMA_RX_CLK1 are each received through an IBUFG. These clocks are then routed onto global clock networks by connecting each to a BUFG. PMA_RX_CLK0 and PMA_RX_CLK1 are each 62.5MHz clocks. Data from the TBI is received alternatively on the rising edge of PMA_RX_CLK0 followed by the rising edge of PMA_RX_CLK1 using IOB Double-Data Rate input registers. This data is then written into the Receiver Elastic Buffer. Data is read out of the Elastic Buffer using the global clock derived from GTX_CLK; all the remaining receiver logic is synchronous to this clock.

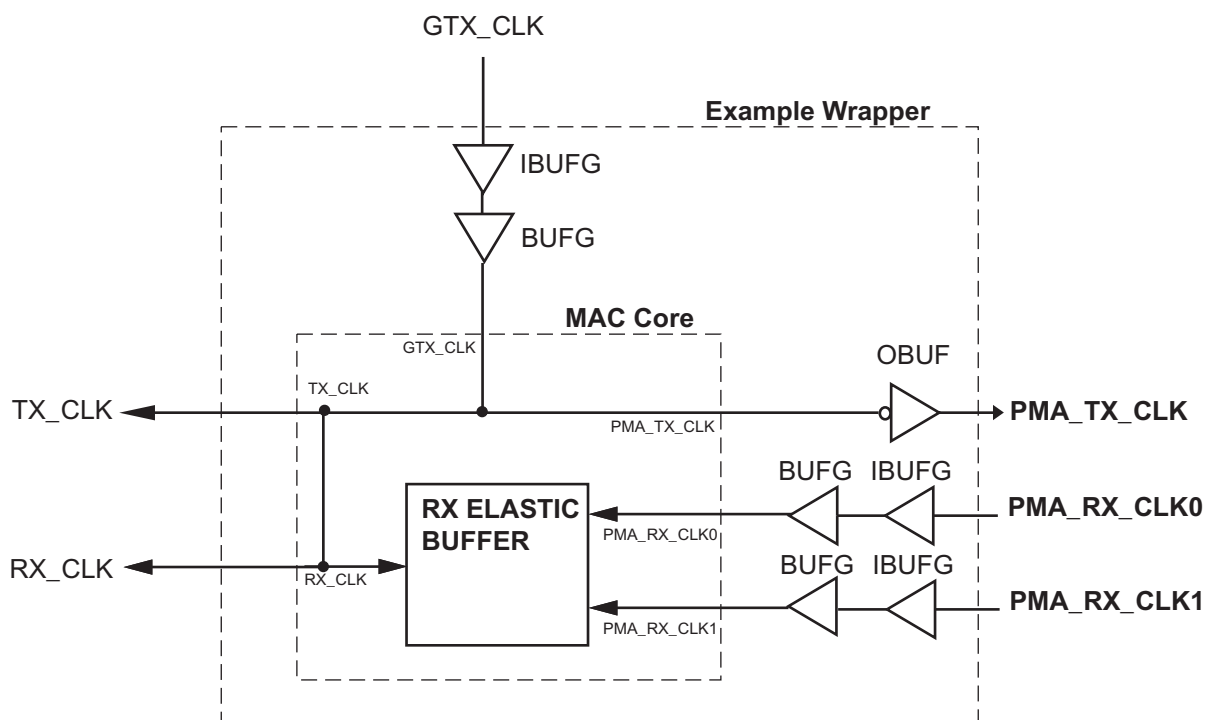


Figure 32: Clock Management for PCS with TBI Interface

Optional PCS and PMA Sublayers for 1000BASE-X (physical_interface=phy)

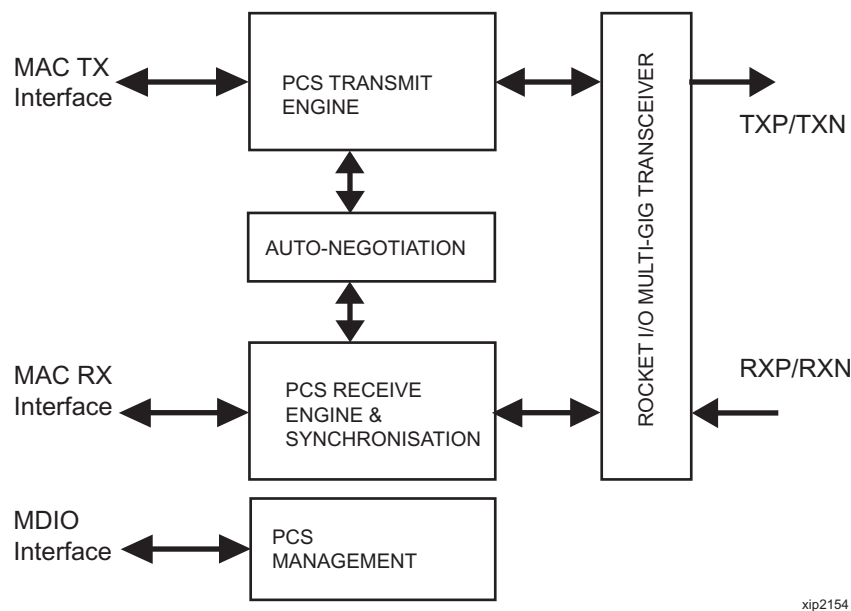
The Full-Duplex Physical Coding Sublayer (PCS) with Physical Medium Attachment (PMA) for 1000BASE-X is defined in IEEE 802.3-2002 Clauses 36 and 37. This functionality is only available in the Virtex-II Pro family of FPGA devices.

A block diagram of the PCS and PMA sublayers can be seen in [Figure 34](#). The functional blocks of the PCS and PMA sublayers may replace the optional GMII interface. The functional blocks of the PCS and PMA sublayers are:

- PCS Transmit Engine
- Auto-Negotiation block
- Receive Engine and Synchronization Block
- PCS Managed Register Block
- Rocket I/O Multi-Gigabit Transceiver

The PCS Managed Register Block is accessed through the MDIO Interface as if it were an externally connected PHY. This configures the operation of the PCS, PMA sublayer, and Auto-Negotiation. See ["PCS Managed Register Block \(physical_interface = tbi or phy\)" on page 49](#). The core's optional Management Interface can be used to control the MDIO Interface as described by ["MDIO Interface" on page 37](#). When the optional Management Interface is not present, the PCS Managed Register Block must be accessed via an MDIO controller which is not provided by the core.

The Rocket I/O Multi-Gigabit Transceiver (MGT) provides some of the PCS layer functionality such as 8B/10B encoding/decoding and the PMA serdes. The remaining PCS functionality such as code group encoding/decoding, the Managed Register Block, and Auto-Negotiation are implemented in CLB logic.



xip2154

Figure 34: Functional Block Diagram of the 1-Gigabit Ethernet PCS/PMA Sublayer Extension

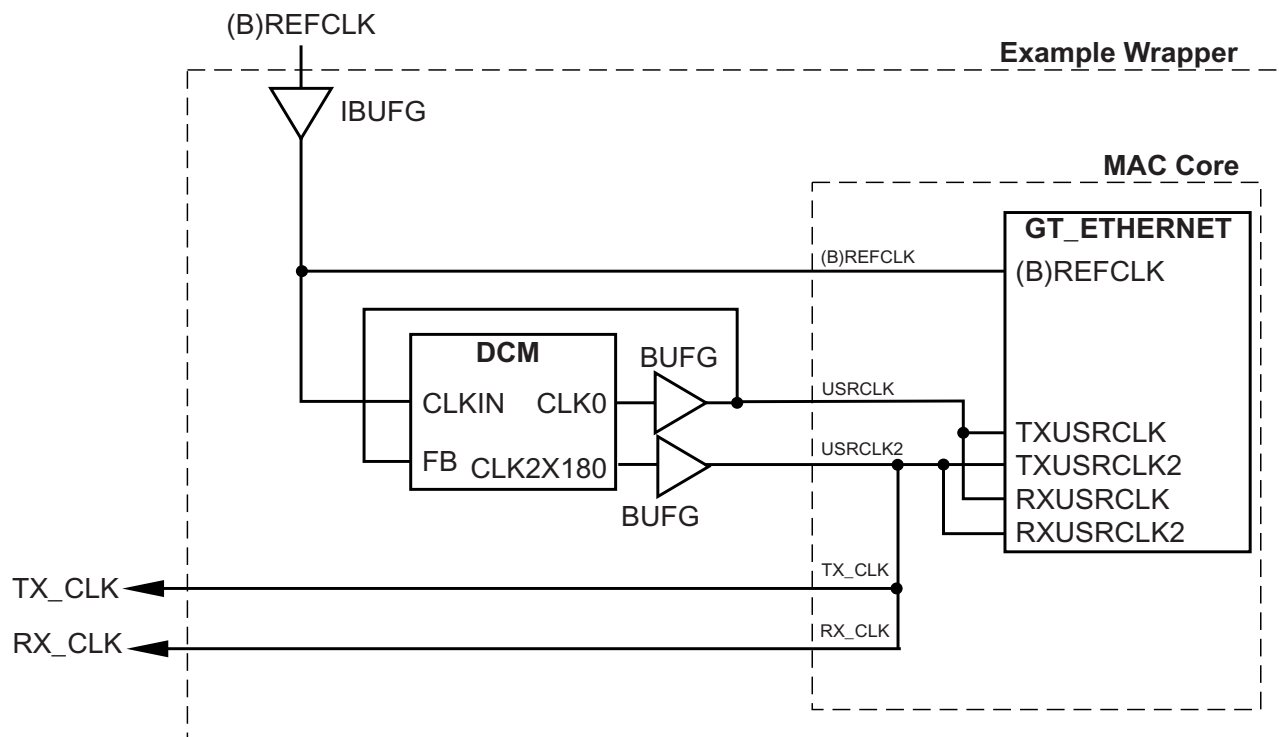
Clock Management

Figure 35 illustrates the clock management that should be used with the optional PCS and PMA sublayers for 1000BASE-X. This logic is implemented in the example wrapper that is delivered with the core. This provides flexibility because the design can be modified to use either REFCLK or BREFCLK (please refer to Rocket I/O documentation). It would also allow multiple instances of the core to share clocks. The example wrapper is provided in both VHDL and Verilog.

(B)REFCLK must be provided to the MAC core. This clock must be derived from an external oscillator and connected to the core through an IBUFG as illustrated. (B)REFCLK is a high quality clock of frequency 62.5 MHz which satisfies the Rocket I/O Multi-Gigabit Transceiver (MGT) requirements.

(B)REFCLK is routed to both the core and a DCM. From the DCM the CLK2X180 output is routed to a BUFG to provide the device with a global 125 MHz clock (connected to USERCLK2 input on the core). Within the core, both TX_CLK and RX_CLK share this global 125 MHz clock source, which is used by all transmitter and receiver logic. This is made possible by the RX_ELASTIC_BUFFER functionality of the Rocket I/O MGT (refer to Virtex-II Pro documentation). The MAC Client can obtain this clock by connecting to either the TX_CLK or the RX_CLK signals output from the core.

From the DCM the CLK0 output is routed to a BUFG to provide the device with a global 62.5MHz clock. This is connected to the USRCLK input of the core.



xip2155

Figure 35: Clock Management with PCS/PMA Sublayers

Clock Sharing between Multiple Cores

Figure 36 illustrates how it is possible to share clock resources across multiple instantiations of the core when using the optional PCS/PMA sublayers. For each core, USERCLK and USERCLK2 must always be derived, as shown, from the BREFCLK or REFCLK used by that core.

Note that when using the fixed routing resources of BREFCLK, Rocket I/O MGTs along the top edge of the device must use a separate BREFCLK routing resource to those along the bottom edge of the device (Refer to Virtex-II Pro documentation).

Although not illustrated, if the optional Management Interface is used, HOST_CLK can also be shared between cores.

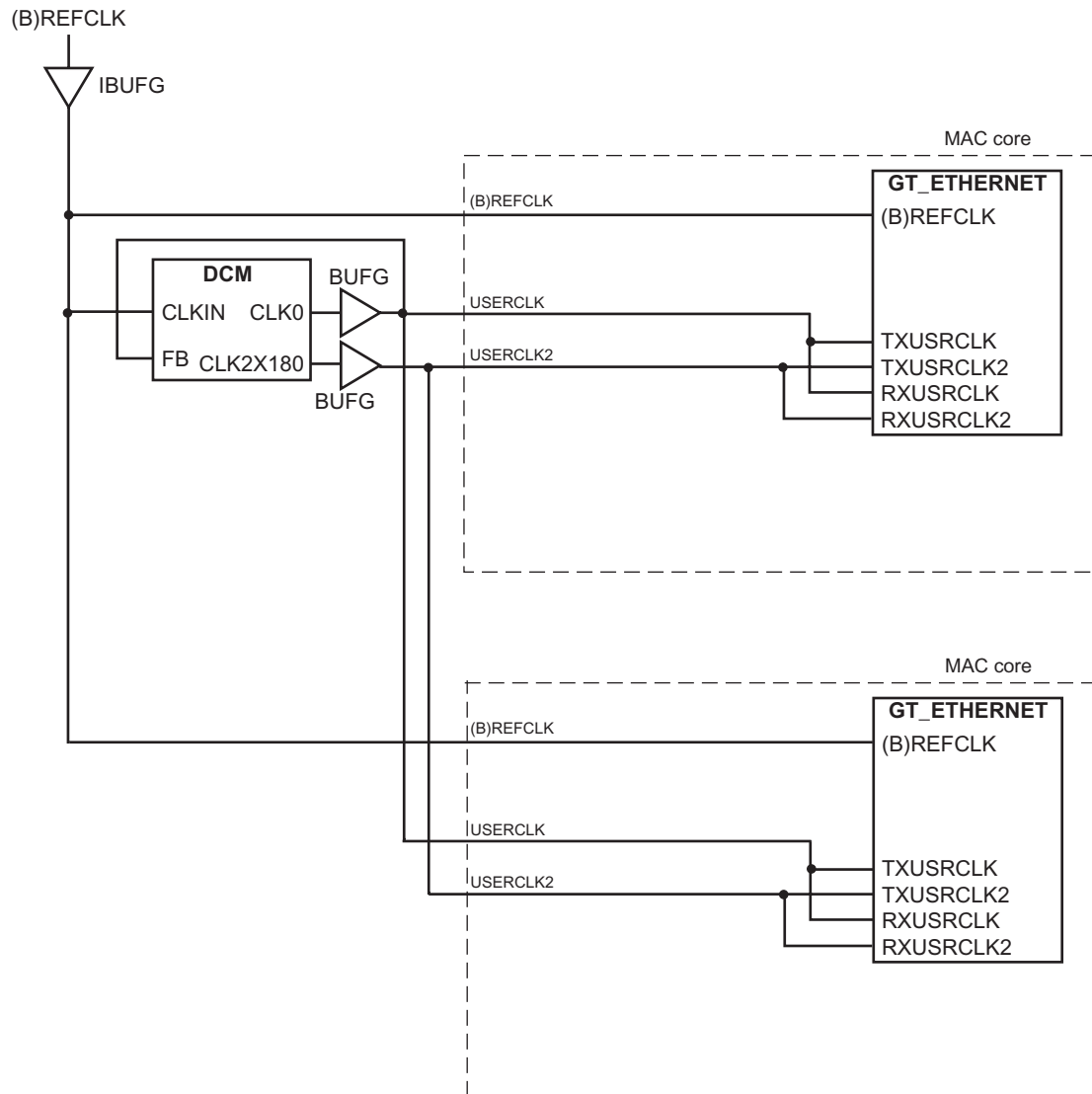


Figure 36: Clock Management with multiple instances of the MAC with PCS and PMA sublayers

Reset circuit

The reset circuits within the MAC when the PCS and PMA sublayers are implemented is the same as that in the GMII case; details of these circuits can be found on [page 42](#).

PCS Managed Register Block (physical_interface = tbi or phy)

The PCS in both the TBI interface and the PCS/PMA (using the Virtex-II Pro Rocket I/O) versions contain the full Managed Register Block defined in IEEE 802.3-2002 clause 37.

This utilizes ten dedicated management registers, accessed via the MDIO interface. These are defined in Table 25 to Table 33, inclusive.

Table 25: Control Register (Register 0)

Bit(s)	Name	Description	Attributes	Default Value
0.15	Reset	1 = PCS/PMA reset. 0 = Normal Operation.	Read/Write Self Clearing	0
0.14	Loopback	1 = Enable Loopback Mode. 0 = Disable Loopback Mode.	Read/Write	0
0.13	Speed Selection (LSB)	The core always returns a 0 for this bit. Together with bit 0.6, speed selection of 1000 Mb/s is identified.	Returns 0	0
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process. 0 = Disable Auto-Negotiation Process.	Read/Write	1
0.11	Power Down	1 = Power down. 0 = Normal operation. When set to "1" the Rocket I/O MGT is placed in a low power state. This bit requires a reset (see bit 0.15) to clear.	Read/ Write	0
0.10	Isolate	1 = Electrically Isolate PHY from GMII. 0 = Normal operation.	Read/Write	1
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process. 0 = Normal Operation.	Read/Write Self Clearing	0
0.8	Duplex Mode	The core always returns a 1 for this bit to signal Full-Duplex Mode.	Returns 1	1
0.7	Collision Test	The core always returns a 0 for this bit to disable COL test.	Returns 0	0
0.6	Speed Selection(MSB)	The core always returns a 1 for this bit. Together with bit 0.13, speed selection of 1000 Mb/s is identified.	Returns 1	1
0.5:0	Reserved	Always returns 0's, writes ignored.	Returns 0's	000000

Table 26: Status Register (Register 1)

Bit(s)	Name	Description	Attributes	Default Value
1.15	100BASE-T4	The core always returns a 0 for this bit because 100BASE-T4 is not supported.	Returns 0	0
1.14	100BASE-X Full Duplex	The core always returns a 0 for this bit because 100BASE-X Full Duplex is not supported.	Returns 0	0
1.13	100BASE-X Half Duplex	The core always returns a 0 for this bit because 100BASE-X Half Duplex is not supported.	Returns 0	0
1.12	10 Mb/s Full Duplex	The core always returns a 0 for this bit because 10 Mb/s Full Duplex is not supported.	Returns 0	0
1.11	10 Mb/s Half Duplex	The core always returns a 0 for this bit because 10 Mb/s Half Duplex is not supported.	Returns 0	0
1.10	100BASE-T2 Full Duplex	The core always returns a 0 for this bit because 100BASE-T2 Full Duplex is not supported.	Returns 0	0
1.9	100BASE-T2 Half Duplex	The core always returns a 0 for this bit because 100BASE-T2 Half Duplex is not supported.	Returns 0	0
1.8	Extended Status	The core always returns a 1 for this bit to indicate the presence of the Extended Register (Register 15).	Returns 1	1
1.7	Reserved	Always return 0, writes ignored.	Returns 0	0
1.6	MF Preamble Suppression	The core always returns a 1 for this bit to indicate that Management Frame Preamble Suppression is supported.	Returns 1	1
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	Read Only	0
1.4	Remote Fault	1 = Remote fault condition detected 0 = No remote fault condition detected	Read Only Self Clearing on read	0
1.3	Auto-Negotiation Ability	The core always returns a 1 for this bit to indicate that the PHY is capable of Auto-Negotiation.	Returns 1	1
1.2	Link Status	1 = Link is up 0 = Link is down	Read Only Self Clearing on read	0
1.1	Jabber Detect	The core always returns a 0 for this bit because Jabber Detect is not supported.	Returns 0	0
1.0	Extended Capability	The core always returns a 0 for this bit because no extended register set is supported.	Returns 0	0

Table 27: PHY Identifier (Registers 2 and 3)

Bit(s)	Name	Description	Attributes	Default Value
2.15:0	Organizationally Unique Identifier	Always returns 0s.	Returns 0s	0000000000000000
3.15:10	Organizationally Unique Identifier	Always returns 0s.	Returns 0s	000000
3.9:4	Manufacturer's model number	Always returns 0s.	Returns 0s	000000
3.3:0	Revision Number	Always returns 0s.	Returns 0s	0000

Table 28: Auto-Negotiation Advertisement Register (Register 4)

Bit(s)	Name	Description	Attributes	Default Value
4.15	Next Page	1 = Next Page functionality is advertised 0 = Next Page functionality is not advertised	Read/Write	0
4.14	Reserved	Always returns 0, writes ignored.	Returns 0	0
4.13:12	Remote Fault	00 = No Error 01 = Offline 10 = Link Failure 11 = Auto-Negotiation Error	Read/Write Self clearing to 00 after Auto-Negotiation	00
4.11:9	Reserved	Always return 0, writes ignored.	Returns 0	0
4.8:7	Pause	00 = No PAUSE 01 = Asymmetric PAUSE towards link partner 10 = Symmetric PAUSE 11 = Both Symmetric PAUSE and Asymmetric PAUSE towards link partner	Read/Write	11
4.6	Half Duplex	The core always returns a 0 for this bit because Half Duplex Mode is not supported.	Returns 0	0
4.5	Full Duplex	1 = Full Duplex Mode is advertised 0 = Full Duplex Mode is not advertised	Read/Write	1
4.4:0	Reserved	Always returns 0s, writes ignored.	Returns 0s	00000

Table 29: Auto-Negotiation Link Partner Ability Base Register (Register 5)

Bit(s)	Name	Description	Attributes	Default Value
5.15	Next Page	1 = Next Page functionality is supported 0 = Next Page functionality is not supported	Read Only	0
5.14	Acknowledge	Used by Auto-Negotiation function to indicate reception of a link partner's base or next page.	Read Only	0
5.13:12	Remote Fault	00 = No Error 01 = Offline 10 = Link Failure 11 = Auto-Negotiation Error	Read Only	00
5.11:9	Reserved	Always returns 0s.	Returns 0s	000
5.8:7	Pause	00 = No PAUSE 01 = Asymmetric PAUSE supported 10 = Symmetric PAUSE supported 11 = Both Symmetric PAUSE and Asymmetric PAUSE supported	Read Only	00
5.6	Half Duplex	1 = Half Duplex Mode is supported 0 = Half Duplex Mode is not supported	Read Only	0
5.5	Full Duplex	1 = Full Duplex Mode is supported 0 = Full Duplex Mode is not supported	Read Only	0
5.4:0	Reserved	Always returns 0s.	Returns 0s	00000

Table 30: Auto-Negotiation Expansion Register (Register 6)

Bit(s)	Name	Description	Attributes	Default Value
6.15:3	Reserved	Always returns 0s.	Returns 0s	00000000000000
6.2	Next Page Able	The core always returns a 1 for this bit because the device is Next Page Able.	Returns 1	1
6.1	Page Received	1 = A new page has been received 0 = A new page has not been received	Read Only Self Clearing on read	0
6.0	Reserved	Always returns 0s.	Returns 0s	0000000

Table 31: Auto-Negotiation Next Page Transmit Register (Register 7)

Bit(s)	Name	Description	Attributes	Default Value
7.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	Read/Write	0
7.14	Reserved	Always returns 0.	Returns 0	0
7.13	Message Page	1 = Message Page 0 = Unformatted Page	Read/Write	1
7.12	Acknowledge 2	1 = Will comply with message 0 = Cannot comply with message	Read/Write	0
7.11	Toggle	Value will toggle between subsequent Next Pages.	Read Only	0
7.10:0	Message / Unformatted Code Field	Message Code Field or Unformatted Page Encoding as dictated by 7.13.	Read/Write	00000000001 (Null Message Code)

Table 32: Auto-Negotiation Next Page Receive Register (Register 8)

Bit(s)	Name	Description	Attributes	Default Value
8.15	Next Page	1 = Additional Next Page(s) follows 0 = Last page	Read Only	0
8.14	Acknowledge	Used by Auto-Negotiation function to indicate reception of a link partner's base or next page.	Read Only	0
8.13	Message Page	1 = Message Page 0 = Unformatted Page	Read Only	0
8.12	Acknowledge 2	1 = Will comply with message 0 = Cannot comply with message	Read Only	0
8.11	Toggle	Value toggles between subsequent and Next Pages.	Read Only	0
8.10:0	Message / Unformatted Code Field	Message Code Field or Unformatted Page Encoding as dictated by 8.13.	Read Only	00000000000

Table 33: Extended Status Register (Register 15)

Bit(s)	Name	Description	Attributes	Default Value
15.15	1000BASE-X Full Duplex	The core always returns a 1 for this bit because 1000BASE-X Full Duplex is supported.	Returns 1	1
15.14	1000BASE-X Half Duplex	The core always returns a 0 for this bit because 1000BASE-X Half Duplex is not supported.	Returns 0	0
15.13	1000BASE-T Full Duplex	The core always returns a 0 for this bit because 1000BASE-T Full Duplex is not supported.	Returns 0	0
15.12	1000BASE-T Half Duplex	The core always returns a 0 for this bit because 1000BASE-T Half Duplex is not supported.	Returns 0	0
15:11:0	Reserved	Always returns 0s.	Returns 0s	000000000000

References

- IEEE 802.3-2002.
- Virtex-E User Guide
- Spartan-II E User Guide
- Virtex-II User Guide
- Virtex-II Pro User Guide

Related Information

Xilinx products are not intended for use in life support appliances, devices, or systems. Use of a Xilinx product in such applications without the written consent of the appropriate Xilinx officer is prohibited.

Ordering Information

This Xilinx LogiCORE module is provided under the [SignOnce IP Site License](#). A free evaluation version of the module is available.

Once purchased, the core may be downloaded from the Xilinx [IP Center](#) for use with the Xilinx CORE Generator System™ v6.1i SP3 and later. The Xilinx CORE Generator System tool is bundled with all Alliance Series Software packages at no additional charge.

Please contact your local Xilinx [sales representative](#) or visit the Xilinx [Silicon Xpresso Cafe](#) for pricing and availability on Xilinx LogiCORE modules and software. Information on additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/03	1.1	Revision History added to document.
04/30/03	2.0	Revised to v3.0 standards.
12/11/03	3.0	Updated to v4.0 release.