Modeling the Short-circuit Energy Dissipation of a CMOS Inverter

Pinar Korkmaz

1. Introduction

The short-circuit energy dissipation results due to a direct path current flowing from the power supply to the ground during the switching of a static CMOS gate. Short-circuit energy constitutes 10-20% of the total energy dissipation of a static CMOS gate [1]. The goal of this work is to develop analytical expressions modeling the short-circuit energy dissipation of a CMOS inverter.

The first closed form expression modeling the short-circuit energy dissipation in a CMOS inverter was developed by Veendrick [2], where zero-load capacitance is assumed. The model results in pessimistic results because of the zero-load capacitance assumption. In addition, the model is based on the Shichman and Hodges square law MOSFET model [3], which ignores the short-channel effects of the submicron devices.

In [4], a more realistic short-circuit energy dissipation model was proposed. This model includes the effect of the output load capacitance. However, the short-channel effects are ignored in the derivation of the model. In [5], the model of [4] is improved by including the velocity saturation effects through use of alpha-power (α-power) law MOS model [6]. However, the contribution of the PMOS (NMOS) currents in falling (rising) output is neglected in the derivation of the model. In addition, the Miller effect of the gate-to-drain capacitance is not included. Also, it is assumed that the load transistor operates only in the saturation region during the time interval in which the short-circuit current flows.

In [7], another short-circuit energy dissipation model based on Shichman and Hodges MOSFET current model was proposed. This model considers the effect of the PMOS (NMOS) current on the short-circuit current in case of the falling (rising) edge of the output through use of two technology dependent empirical parameters. The Miller effect of the gate-to-drain capacitance is also included in the model. To include this effect, technology dependent empirical parameters are used.

In [8], the short-circuit current waveform was approximated with a piecewise linear function of the time to estimate the short-circuit energy dissipation. In this model, the energy dissipation of the reverse current due to the gate-to-drain capacitance is subtracted from the short-circuit energy dissipation. However, this reverse current is provided from the inverter input, but not from the power supply of the gate, hence this energy component can not be included in the short-circuit energy dissipation.

In [9], a short-circuit model was developed using α-power law MOS model [6]. The model takes into account the current through both transistors. The influence of the gate-to-drain capacitances of both transistors and the gate-to-source capacitance of the short circuiting transistor are included in the derivation of the model. However, the α-power law MOS model does not very well capture the short-channel effects.

Nose and Sakurai [10] derived a closed-form expression for modeling the short-circuit energy dissipation of a CMOS inverter. They used an alpha-power law MOSFET model [11] in their derivation, which is more accurate especially in the triode region [12] than the original alpha-power law model [6]. Their model includes the short-channel effects. However, the model does not include the effect of the gate-drain and gate-source capacitance of the transistors.

In this work, we improve the model in [9] by using the alpha power law MOS model of [10].

2. Modeling the Short-circuit Energy Dissipation of a CMOS Inverter

In this section, we derive the short-circuit energy dissipation in a CMOS inverter (shown in Figure 1) for the rising input. The derivation for the falling input can be carried out in a similar way.

In Figure 1, the output capacitance C_o includes the drain junction capacitances of the two transistors of the inverter, the gate capacitances of the fan-out gates, and the interconnect capacitance. C_M is the Miller capacitance and is equal to the sum of the gate to drain capacitance of both transistors. C_{gsp} is the gate to source capacitance of the PMOS transistor. I_p and I_n are the drain to source currents of the PMOS and NMOS transistors respectively.

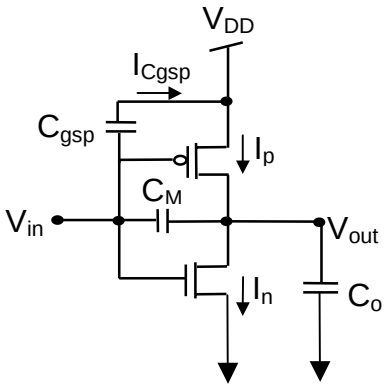

Figure 1. The CMOS inverter

The input, V_{in}, is represented by $V_{in} = V_{DD}.(t/\tau)$ for $0 \le t \le \tau$, where τ is the input rise time. The differential equation in (1) describes the discharge of the output capacitance C_o.

$$C_o \frac{dV_{out}}{dt} = C_m\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) + I_p - I_n \qquad (1)$$

To calculate the currents I_p and I_n, we use the α-power law MOSFET current model [10] provided below in (2). The model consists of four parameters, α, I_{DO}, V_{DO} and V_{TH}. α represents the velocity saturation index which is an empirical parameter. I_{DO} is the drain current at $V_{GS} = V_{DS} = V_{DD}$. V_{DO} is the drain to source saturation voltage at $V_{GS} = V_{DD}$. V_{TH} represents the threshold voltage and it is not the same as the physical threshold (V_{th}) of the transistor.

$$I_p = \begin{cases} 0, & |V_{GS}| < V_{THP} \text{ (cutoff region)} \\ I_{D_p} \cdot \left(2 - \dfrac{|V_{DS}|}{V_{D_p}}\right)\dfrac{|V_{DS}|}{V_{D_p}}, & |V_{DS}| < V_{D_p} \text{ (linear region)} \\ I_{D_p}, & |V_{DS}| < V_{D_p} \text{ (saturation region)} \end{cases} \tag{2}$$

where

$$\begin{aligned} I_{D_p} &= I_{DOP}\left(\frac{|V_{GS}| - V_{THP}}{V_{DD} - V_{THP}}\right)^{\alpha_p} \\ V_{D_p} &= V_{DOP}\left(\frac{|V_{GS}| - V_{THP}}{V_{DD} - V_{THP}}\right)^{\alpha_p/2} \end{aligned} \tag{3}$$

The NMOS device current is

$$I_n = \begin{cases} 0, & V_{GS} < V_{THN} \text{ (cutoff region)} \\ I_{D_n} \cdot \left(2 - \dfrac{V_{DS}}{V_{D_n}}\right)\dfrac{V_{DS}}{V_{D_n}}, & V_{DS} < V_{D_n} \text{ (linear region)} \\ I_{D_n}, & V_{DS} < V_{D_n} \text{ (saturation region)} \end{cases} \tag{4}$$

where

$$\begin{aligned} I_{D_n} &= I_{DON}\left(\frac{V_{GS} - V_{THN}}{V_{DD} - V_{THN}}\right)^{\alpha_n} \\ V_{D_n} &= V_{DON}\left(\frac{V_{GS} - V_{THN}}{V_{DD} - V_{THN}}\right)^{\alpha_n/2} \end{aligned} \tag{5}$$

To calculate the short-circuit energy dissipation; we first derive the analytical expressions of the output voltage waveforms of the CMOS inverter. Figure 2 shows the input and output voltage waveforms and the operating regions for the rising input.

In region 1 ($0 \le t \le t_n$), the NMOS transistor is OFF and the PMOS transistor is in the linear region. Thus, the NMOS and PMOS currents are as follows

$$\begin{aligned} I_n &= 0 \\ I_p &= I_{D_p} \cdot \left(2 - \frac{V_{DD} - V_{out}}{V_{D_p}}\right)\left(\frac{V_{DD} - V_{out}}{V_{D_p}}\right), \quad |V_{DS}| < V_{D_p} \end{aligned} \tag{6}$$

Then, the differential equation in (1) can be expressed as

$$\frac{dV_{out}}{dt} = AV_{out}^2 + BV_{out} + C \tag{7}$$

where

$$\begin{aligned} A &= -\frac{I_{D_{ph}}}{(C_L + C_M)V_{D_p}^2} \\ B &= -\frac{2I_{D_{ph}}\left(V_{D_{ph}} - V_{DD}\right)}{(C_L + C_M)V_{D_{ph}}^2} \\ C &= \frac{C_M}{(C_L + C_M)}\frac{V_{DD}}{\tau} - \frac{I_{D_{ph}}V_{DD}^2}{(C_L + C_M)V_{D_{ph}}^2} + \frac{2I_{D_{ph}}V_{DD}}{(C_L + C_M)V_{D_{ph}}} \end{aligned} \tag{8}$$

To derive (8), I_{D_p} and V_{D_p} are approximated to be constant and equal to $I_{D_{ph}}$ and $V_{D_{ph}}$ respectively. $I_{D_{ph}}$ and $V_{D_{ph}}$ correspond to the values of I_{D_p} and V_{D_p} in the middle of the interval ($0 \le t \le t_n$) and are expressed as follows

$$\begin{aligned} I_{D_{ph}} &= I_{DOP}\left(\frac{V_{DD} - V_{THN}/2 - V_{THP}}{V_{DD} - V_{THP}}\right)^{\alpha_p} \\ V_{D_{ph}} &= V_{DOP}\left(\frac{V_{DD} - V_{THN}/2 - V_{THP}}{V_{DD} - V_{THP}}\right)^{\alpha_p/2} \end{aligned} \tag{9}$$

The differential equation (7) is a Verhulst equation [13]. It is solved using the condition $V_{out}(0) = V_{DD}$ and the solution is described by

$$V_{out}(t) = K_1 + \frac{1}{\frac{A}{E}\left(e^{-Et} - 1\right) + \frac{e^{-Et}}{V_{DD} - K_1}} \tag{10}$$

where

$$E = \sqrt{B^2 - 4AC} \tag{11}$$

and

$$K_1 = \frac{E - B}{2A} \tag{12}$$

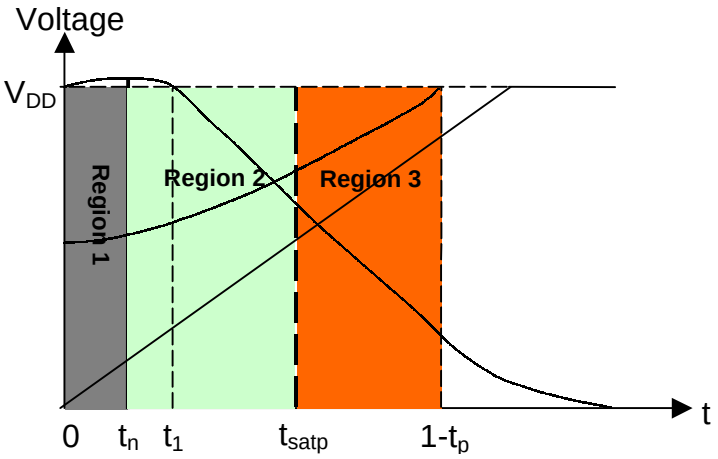

Figure 2. Operating regions of the CMOS inverter during a rising input

As shown in Figure 2, there is an overshoot at the early part of the output voltage ($0 \le t \le t_1$), that is, the output voltage is greater than the supply voltage. During the overshoot, there is no current flowing from the power supply to the ground. Hence, the short-circuit power consumption is zero during the overshoot.

In region 2 ($t_n \le t \le t_{satp}$), the NMOS transistor is saturated and the PMOS transistor is in the linear region. t_{satp} represents the point in time when the PMOS transistor enters the saturation region. In this region, the PMOS current is approximated by a linear function of time as demonstrated in Figure 3. The approximation is shown in (13).

$$I_p = I_{p_{\min}} + S\left(t - \frac{V_{THN}}{V_{DD}}\tau\right) \tag{13}$$

I_{pmin} represents the value of the PMOS current at $t_n = \frac{V_{THN}}{V_{DD}}\tau$. t_n is the point in time when the NMOS transistor leaves the cutoff region and enters the saturation region. The value of the output voltage at t_n is (using (10))

$$V_{out}(t_n) = K_1 + \frac{1}{\frac{A}{E}\left(e^{-Et_n} - 1\right) + \frac{e^{-Et_n}}{V_{DD} - K_1}} \tag{14}$$

and I_{pmin} is described by (using (6))

$$I_{p\min} = I_{Dp}\Big|_{t=t_n} \cdot \left(2 - \frac{V_{DD} - V_{out}(t_n)}{V_{Dp}\Big|_{t=t_n}}\right)\left(\frac{V_{DD} - V_{out}(t_n)}{V_{Dp}\Big|_{t=t_n}}\right) \tag{15}$$

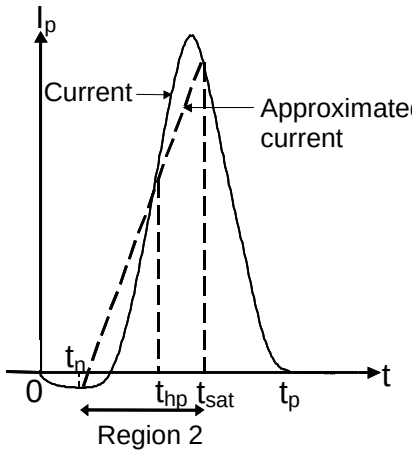

Figure 3. Linear approximation of PMOS current in region 2

In region 2, the NMOS transistor current is given by

$$I_n = I_{DON}\left(\frac{V_{DD}\dfrac{t}{\tau} - V_{THN}}{V_{DD} - V_{THN}}\right)^{\alpha_n} \tag{16}$$

Replacing (13) and (16) for I_p and I_n in (1), the output voltage waveform in region 2 is calculated and found to be described by the following expression

$$V_{out}(t) = A_2\left(t - \frac{V_{THN}}{V_{DD}}\right)^{\alpha_n+1} + B_2 t^2 + C_2 t + K \tag{17}$$

where

$$\begin{aligned}
A_2 &= -\frac{I_{DON}}{(C_L + C_M)(\alpha_N + 1)}\left(\frac{V_{DD}}{\tau(V_{DD} - V_{THN})}\right)^{\alpha_N} \\
B_2 &= \frac{S}{2(C_L + C_M)} \\
C_2 &= \frac{C_M}{(C_L + C_M)}\frac{V_{DD}}{\tau} + \frac{V_{DD} I_{p\min} - S\tau V_{THN}}{V_{DD}(C_L + C_M)} \\
K &= V_{out}(t_n) + \frac{S V_{THN}^2 \tau}{2(C_L + C_M)V_{DD}^2} - \frac{C_M}{(C_L + C_M)}V_{THN} - \frac{\tau V_{THN} I_{p\min}}{V_{DD}(C_L + C_M)}
\end{aligned} \tag{18}$$

The slope of the PMOS current waveform, S, is calculated by equating the PMOS current in linear region (using (6)) to the approximated current (using (13)) at time $t_{hp} = \frac{\tau}{2} - \frac{V_{THP}\tau}{2V_{DD}}$.

At $t = t_{satp}$, the PMOS transistor is entering the saturation region. Hence, at time $t = t_{satp}$, the following saturation condition is satisfied

$$V_{out} = V_{DD} - V_{D_p} \tag{19}$$

To find t_{satp}, we use a Taylor series expansion around the point $t = \tau - \frac{\tau}{V_{DD}}(V_{THP} + V_{THN})$ up to the second order coefficient, for both V_{out} and V_{D_p} (in (19)). t_{satp} is expressed as

$$t_{satp} = \frac{-E_2 + \sqrt{E_2^2 - 4D_2F_2}}{2D_2} \tag{20}$$

where

$$\begin{aligned} D_5 &= A_2A_3 + B_2 + A_4V_{DOP} \\ E_5 &= A_2B_3 + V_{DOP}B_4 + C_2 \\ F_5 &= A_2C_3 + K + V_{DOP}C_4 - V_{DD} \end{aligned} \tag{21}$$

with

$$\begin{aligned} A_3 &= \frac{\alpha_n(\alpha_n+1)}{2}\left(\frac{\tau(V_{DD}-V_{THP}-2V_{THN})}{V_{DD}}\right)^{\alpha_n-1} \\ B_3 &= (\alpha_n+1)\left(\frac{\tau(V_{DD}-V_{THP}-2V_{THN})}{V_{DD}}\right)^{\alpha_n}\left(1-\alpha_n\left(\frac{V_{DD}-V_{THP}-V_{THN}}{V_{DD}-V_{THP}-2V_{THN}}\right)\right) \\ C_3 &= \left(\frac{\tau(V_{DD}-V_{THP}-2V_{THN})}{V_{DD}}\right)^{\alpha_n+1}\left(\begin{array}{l} 1-(\alpha_n+1)\left(\frac{V_{DD}-V_{THP}-V_{THN}}{V_{DD}-V_{THP}-2V_{THN}}\right) \\ +\frac{\alpha_n(\alpha_n+1)}{2}\left(\frac{V_{DD}-V_{THP}-V_{THN}}{V_{DD}-V_{THP}-2V_{THN}}\right)^2 \end{array}\right) \\ A_4 &= \frac{\alpha_p}{4}\left(\frac{\alpha_p}{2}-1\right)\left(\frac{V_{DD}}{\tau V_{THN}}\right)^2\left(\frac{V_{THN}}{V_{DD}-V_{THP}}\right)^{\frac{\alpha_p}{2}} \\ B_4 &= -\frac{\alpha_p}{2}\cdot\frac{V_{DD}}{\tau V_{THN}}(V_{THN})^{\frac{\alpha_p}{2}}\left(1-\left(\frac{\alpha_p}{2}-1\right)\frac{V_{THN}+V_{THP}-V_{DD}}{V_{THN}}\right) \\ C_4 &= \left(\frac{V_{THN}}{V_{DD}-V_{THP}}\right)^{\frac{\alpha_p}{2}}\left(\begin{array}{l} 1-\frac{\alpha_p}{2}\cdot\frac{V_{THN}+V_{THP}-V_{DD}}{V_{THN}}+ \\ \frac{\alpha_p}{4}\left(\frac{\alpha_p}{2}-1\right)\left(\frac{V_{THN}+V_{THP}-V_{DD}}{V_{THN}}\right)^2 \end{array}\right) \end{aligned} \tag{22}$$

Referring to Figure 2, t_1 corresponds to the point in time when the output voltage overshoot finishes. It is calculated by solving the equation $V_{out} = V_{DD}$, using the Taylor series expansion of V_{out} around the point $t = \frac{3}{2}\frac{\tau V_{THN}}{V_{DD}}$. Note that in [9], a Taylor series expansion around $t = 2\frac{\tau V_{THN}}{V_{DD}}$ is used. However, our HSpice simulations show that t_1 is closer to $t = \frac{3}{2}\frac{\tau V_{THN}}{V_{DD}}$. Then, t_1 is described by

$$t_1 = \frac{-E_6 + \sqrt{E_6^2 - 4D_6F_6}}{2D_6} \tag{23}$$

where

$$\begin{aligned} D_6 &= A_2A_5 + B_2 \\ E_6 &= A_2B_5 + C_2 \\ F_6 &= A_2C_5 + K - V_{DD} \end{aligned} \tag{24}$$

and

$$\begin{aligned} A_5 &= \frac{\alpha_n(\alpha_n+1)}{2}\left(\frac{\tau V_{THN}}{2V_{DD}}\right)^{\alpha_n-1} \\ B_5 &= (\alpha_n+1)\left(\frac{\tau V_{THN}}{2V_{DD}}\right)^{\alpha_n}(1-3\alpha_n) \\ C_5 &= \left(\frac{\tau V_{THN}}{2V_{DD}}\right)^{\alpha_n+1}\left(1-3(\alpha_n+1)+\frac{9}{2}\alpha_n(\alpha_n+1)\right) \end{aligned} \tag{25}$$

In region 3 ($t_{satp} \le t \le t_p$), both of the transistors are saturated. Hence, the PMOS and NMOS currents are described as

$$\begin{aligned} I_p &= I_{DOP}\left(\frac{V_{DD} - V_{DD}\frac{t}{\tau} - V_{THP}}{V_{DD} - V_{THP}}\right)^{\alpha_p} \\ I_n &= I_{DON}\left(\frac{V_{DD}\frac{t}{\tau} - V_{THN}}{V_{DD} - V_{THN}}\right)^{\alpha_n} \end{aligned} \tag{26}$$

Note that t_p corresponds to the point in time when the PMOS transistor enters the cutoff region.

Referring to Figure 1, the short-circuit current I_{sc} (during a rising input) is expressed as

$$I_{sc} = I_p - I_{C_{gsp}} \tag{27}$$

The current $I_{C_{gsp}}$ is given by

$$I_{C_{gsp}} = C_{gsp} \frac{dV_{in}}{dt} = C_{gsp} \frac{V_{DD}}{\tau} \tag{28}$$

The short-circuit energy dissipation occurs in the interval $[t_2, t_3]$ since there is a path from the power supply to the ground in this interval, and is defined as

$$E_{sc}^{r} = V_{DD} \int_{t_2}^{t_3} I_{sc} dt = V_{DD} \left(\int_{t_2}^{t_{sat}} I_{sc} dt + \int_{t_{sat}}^{t_3} I_{sc} dt \right) \tag{29}$$

As shown in Figure 4, I_{sc} is negative until t_2 (when it becomes zero). In addition, t_3 represents the point in time when I_{sc} becomes zero again when the PMOS transistor enters the cutoff region.

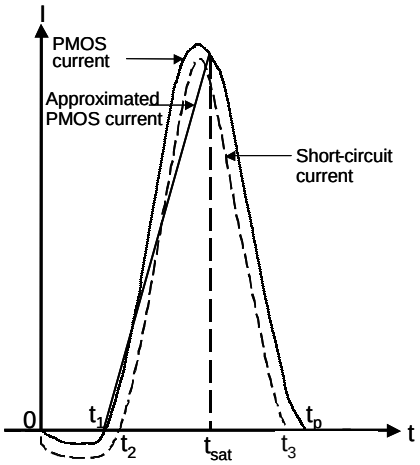

Figure 4. PMOS and short-circuit current waveforms of the inverter

In the first integral of (29), a linear approximation of the PMOS transistor current is used

$$I_p = S'(t - t_1) \tag{30}$$

where S$^{'}$ is the slope of I_p (Figure 4) and calculated by equating the PMOS current in linear region (using (6)) to the approximated current (using (29)) at time $t = \frac{t_1 + t_{satp}}{2}$.

In the second interval of (29), the PMOS is in saturation region and I_p is given by (2). Then, E_{sc}^r is described by

$$E_{sc}^r = \frac{V_{DD}(t_{sat} - t_2)}{2}\left(\left(S'(t_{satp} + t_2) - 2S't_1\right) - \frac{2C_{gsp}V_{DD}}{\tau}\right) - \frac{V_{DD}I_{DOP}}{(V_{DD} - V_{THP})^{\alpha^p}}\left(\left(\frac{V_{DD}t_3}{\tau} - V_{THP}\right)^{\alpha_p+1} - \left(\frac{V_{DD}t_{satp}}{\tau} - V_{THP}\right)^{\alpha_p+1}\right) - \frac{V_{DD}^2 C_{gsp}}{\tau}(t_3 - t_{satp}) \quad (31)$$

The value of t_2 is given by

$$t_2 = t_1 + C_{gsp}\frac{V_{DD}}{S'\tau} = 0 \quad (32)$$

The value of t_3 is calculated by the equation

$$I_{DOP}\left(\frac{\tau}{(V_{DD} - V_{THP})V_{DD}}\right)^{\alpha_p}\left(t - \frac{V_{THP}\tau}{V_{DD}}\right)^{\alpha_p} - C_{gsp}\frac{V_{DD}}{\tau} = 0 \quad (33)$$

We use a Taylor series expansion of the term $(t - V_{THP}\tau / V_{DD})^{\alpha_p}$ around the point $t = \frac{t_{satp}}{4} + \frac{3\tau}{4}\left(1 - \frac{V_{THP}}{V_{DD}}\right)$ up to the second coefficient to solve (33). t_3 is described as follows

$$t_3 = \frac{-E_7 + \sqrt{E_7^2 - 4D_7F_7}}{2D_7} \quad (34)$$

where

$$D_7 = \frac{I_{DOP}A_6}{(V_{DD} - V_{THP})^{\alpha_p}}\left(\frac{V_{DD}}{\tau}\right)^{\alpha_p}$$
$$E_7 = \frac{I_{DOP}B_6}{(V_{DD} - V_{THP})^{\alpha_p}}\left(\frac{V_{DD}}{\tau}\right)^{\alpha_p} \quad (35)$$
$$F_6 = \frac{I_{DOP}C_6}{(V_{DD} - V_{THP})^{\alpha_p}}\left(\frac{V_{DD}}{\tau}\right)^{\alpha_p} - \frac{C_{gsp}V_{DD}}{\tau}$$

with

$$
\begin{aligned}
A_6 &= \frac{\alpha_p(\alpha_p-1)}{2}\left(\frac{V_{DD}}{\tau}\right)^2\left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{\alpha_p-2}\\
B_6 &= -\frac{\alpha_p V_{DD}}{\tau}\left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{\alpha_p-1}\\
&\quad\times\left(1-(\alpha_p-1)\frac{V_{DD}}{\tau}\left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{-1}\left(-\frac{t_{satp}}{4}-\frac{3\tau}{4}+\frac{3\tau}{4}\frac{V_{THP}}{V_{DD}}\right)\right)\\
C_6 &= \left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{\alpha_p}\\
&\times\left(\begin{array}{l}1-\alpha_p\frac{V_{DD}}{\tau}\left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{-1}\left(-\frac{t_{satp}}{4}-\frac{3\tau}{4}+\frac{3\tau}{4}\frac{V_{THP}}{V_{DD}}\right)\\ +\frac{\alpha_p(\alpha_p-1)}{2}\left(\frac{V_{DD}}{\tau}\right)^2\left(-\frac{V_{DD}\cdot t_{satp}}{4\tau}+\frac{V_{DD}-V_{THP}}{4}\right)^{-2}\left(-\frac{t_{satp}}{4}-\frac{3\tau}{4}+\frac{3\tau}{4}\frac{V_{THP}}{V_{DD}}\right)^2\end{array}\right)
\end{aligned}
\tag{36}
$$

The short-circuit energy consumption during the falling transition of the input can be evaluated symmetrically and is expressed as follows:

$$
\begin{aligned}
E_{sc}^{f} &= \frac{V_{DD}(t_{satn}-t_2)}{2}\left(\left(S'(t_{satn}+t_2)-2S't_1\right)-\frac{2C_{gsn}V_{DD}}{\tau}\right)-\frac{V_{DD}I_{DON}}{(V_{DD}-V_{THN})^{\alpha_n}}\times\\
&\left(\left(\frac{V_{DD}t_3}{\tau}-V_{THN}\right)^{\alpha_n+1}-\left(\frac{V_{DD}t_{satn}}{\tau}-V_{THN}\right)^{\alpha_n+1}\right)-\frac{V_{DD}^2C_{gsn}}{\tau}(t_3-t_{satn})
\end{aligned}
\tag{31}
$$

3. Model Validation

In this section, we illustrate the validity of the analytical model for the short-circuit energy dissipation of the static inverter through comparison of the analytical results to the results of circuit simulations in HSpice. The comparisons are done for a TSMC 0.25μm CMOS technology.

Figure 5 shows the comparison between the calculated and the simulated results of the short-circuit energy consumption of a TSMC 0.25μm inverter with a supply voltage value of 2.5V as a function of the input transition time τ. A capacitive load of 130fF is used for the calculations and the simulations. Table 1 shows the MOSFET model parameters used

in the calculations. In simulations, we use level 49 HSpice model parameters for the TSMC 0.25μm transistors. It can be observed from Figure 5 that, our results are very close to the results derived from HSpice simulations. The maximum error is 12.23 % and the average error 7.416 %.

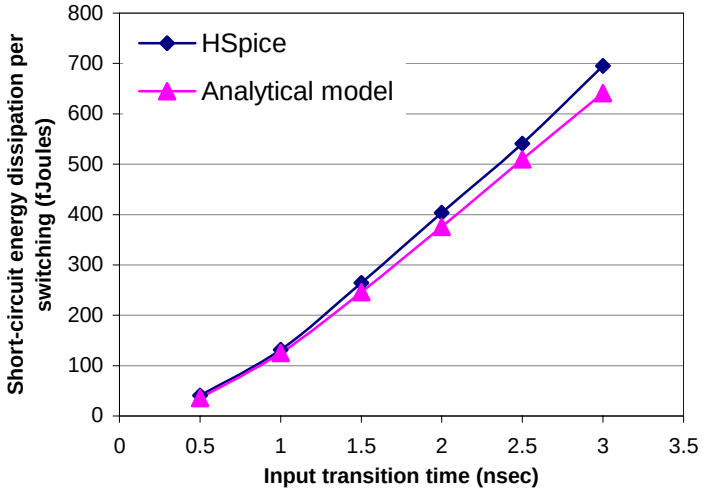

Figure 5. TSMC 0.25μm inverter short-circuit energy dissipation during switching as a function of the input transition time

Table I
MOSFET model parameters used in the analytical model

	NMOS	PMOS
W(μm)	3.36	6.72
L(μm)	0.25	0.25
α	1.07	1.167
I_{DO}(mA)	1.98	1.87
$\|V_{DO}\|$ (V)	1.167	1.99
$\|V_{TH}\|$ (V)	0.67	0.63
C_{gs} (fF)	6	9
C_{gd} (fF)	7.5	12.5

Figure 6 shows the comparison between the calculated and the simulated results of the short-circuit energy consumption of a TSMC 0.25μm inverter as a function of the input transition time τ for two different values of load capacitance (200fF and 50fF). The value of the supply voltage is 2.5V. The figure shows that the short-circuit energy consumption decreases with increasing load capacitance.

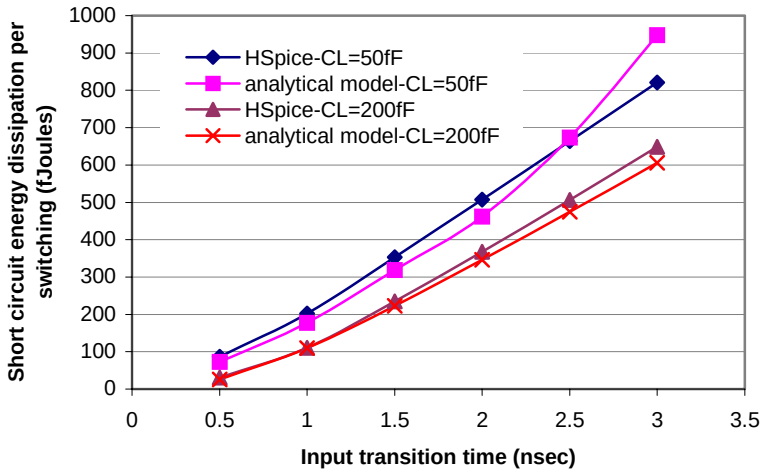

Figure 6. TSMC 0.25µm inverter short-circuit energy dissipation during switching as a function of the input transition time for load capacitance values of 50fF and 200fF

Figure 7 shows the simulation and calculated results for a TSMC 0.25µm inverter as a function of the supply voltage. In addition, the figure illustrates a comparison of our analytical model to the model developed in [9] (which we refer to as the Bisdounis model in the figure). The capacitive load is 150fF and the input transition time is 2nsec. The average error of our analytical model, 5.547% is smaller than the average error, 10.674%, of the Bisdounis model. This results from using a more accurate MOSFET current model as we discussed before in Section 1.

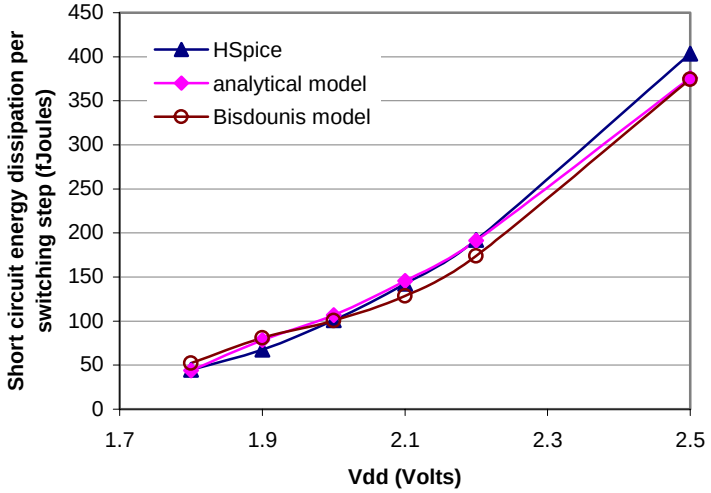

Figure 7. TSMC 0.25µm inverter short-circuit energy dissipation as a function of the supply voltage

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