Krishna V. Palem

I. RESEARCH INTERESTS

Adaptive and reconfigurable computing, Algorithms, Applied Probability, Compiler optimizations, Embedded systems, Low energy computing, Nano-scale Electronics and Computing, Technology for societal benefits

II. EARNED DEGREES

University of Texas, Austin, TX
Ph.D., August 1986

University of Texas, Austin, TX
M.S. in Electrical and Computer Engineering (Biomedical Engineering), August 1981

III. EMPLOYMENT

Jan 2010 – Present	**Rice University – Nanyang Technological University, Singapore** *Director, NTU-Rice Institute on Sustainable and Applied Infodynamics (ISAID)*
Aug 2007 – Present	**Rice University** *Kenneth and Audrey Kennedy Professor of Computing* *Professor, Computer Science, Electrical and Computer Engineering, Statistics* *Baker Institute Rice Scholar*
Aug 2008 – Dec 2009	**Nanyang Technological University** *Director, ISNE*
2000 – 2007	**Georgia Institute of Technology** *Professor of Electrical & Computer Engineering* *Professor of Computer Science, College of Computing* *Senior Research Leader (funded), College of Engineering* *Director, Center for Research in Embedded Systems and Technology*
Dec 1999 – July 2003	**Proceler Inc.** *Co-founder and Chief Technology Officer*

1994 – Dec 1999	**New York University** *Associate Professor, Courant Institute of Mathematical Sciences*
1986 – 1994	**IBM T. J. Watson Research Center** *Research Staff Member*
1991 – 1994	**IBM Santa Teresa Laboratory** *Advanced Technology Consultant*
1989 – 1993	**New York University** *Visiting Member, Courant Institute*
1991 – 1994	**Stanford University** *Visiting Scholar, Computer Science Department*

IV. SELECTED RECOGNITION AND VISITING FELLOWSHIPS

Awards and Fellowships

1. IEEE W. Wallace McDowell Award, *highest technical award made solely by the IEEE Computer Society*[1] for "pioneering contributions to the algorithmic, compilation, and architectural foundations of embedded computing", 2008.

2. *Moore Distinguished Faculty Fellow*, California Institute of Technology, 2006–07.

3. Best paper award for Jason George, Bo Marr, Bilge E. S. Akgul and Krishna V. Palem, "Probabilistic Arithmetic and Energy Efficient Embedded Signal Processing", *Proceedings of the ACM-IEEE Intl. Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, 2006.

4. Fellow of the ACM for "contributions to compiler optimization and embedded computing", 2005.

5. Fellow of the IEEE for "contributions to embedded computing", 2004.

6. *Invited Professor*, Ecole Normale Superieure, Paris, France, 2004 – 05.

7. *Schonbrunn Fellow*, The Hebrew University, Jerusalem, Israel, 2000.

8. *Teaching Excellence*, The Hebrew University, Jerusalem, Israel, 2000.

[1] http://www.isaid.rice.edu/files/wallace.pdf

Industrial and Technology Recognition

1. I-Slate, one of *Seven World-Changing Technologies*[2], featured as part of IEEE's 125th Anniversary, 2009; supported by

    a. Krishna V Palem, Avinash Lingamneni, and Lakshmi Chakrapani, "Device using inexact computing architecture processor," US Patent, pending App. No. 61/158,663, USA.
    b. Krishna V Palem, Al Barr, Avinash Lingamneni, Vincent Mooney, Rajeswari Pingali, Harini Sampath, and Jayanthi Sivaswamy, "I-Slate, Ethnomathematics and Rural Education," *IEEE Conference on Technologies for Humanitarian Challenges, 2009.*

2. Probabilistic Chips (PCMOS), one of *10 technologies that we think are most likely to change the way we live*[3], Technology Review published by MIT, 2008; supported by

    a. Krishna V. Palem, Suresh Cheemalavagu, Pinar Korkmaz, and Bilge E. Akgul, "Probabilistic And Introverted Switching To Conserve Energy In A Digital System," United States Patent 7290154.
    b. Krishna V. Palem, "Energy Aware Computing Through Probabilistic Switching: A Study of Limits," *IEEE Transactions on Computers*, 54(9), pp. 1123-1137, September 2005.

3. Proceler Inc's Architecture Assembly nominee (one of four) for *Analysts' Choice Award for Outstanding Technology in the field of Digital Processing, 2001*[4] ; supported by

    a. Max Baron,"Technology 2001: On a clear day you can see forever," Microprocessor Report, 2002.
    b. H. Patel, Krishna V Palem, and S. Yalamanchili, "Parameterized Application Programming Interface for Reconfigurable Computing Systems," Patent Application: US Serial No. 09/860,942.
    c. Krishna V Palem, H. Patel, and S. Yalamanchili, "An Instruction Set Architecture to Aid Code Generation for Hardware Platforms Multiple Heterogeneous Functional Units," Patent Application: US Serial No. 09/715,578.
    d. S. Talla, P. Devaney, and Krishna V Palem "Adaptive Explicitly Parallel Instruction Computing," *Fourth Australasian Computer Architecture Conference*, Auckland, New Zealand, January 1999.

4. *External Recognition Award*, IBM Research Division, 1994.

Student Supervision Awards

1. L. Chakrapani, *Sigma Xi Best Dissertation Award*, ``Probabilistic Boolean Logic, Arithmetic and Architectures, August 2008, Georgia Tech.

[2] http://www.isaid.rice.edu/files/ieee.pdf
[3] http://www.technologyreview.com/specialreports/specialreport.aspx?id=25
[4] http://www.rose-hulman.edu/class/ee/yoder/ece332/Papers/Technology2001ClearDay.pdf

2. S. Talla, *Janet Fabri Award for Outstanding Doctoral Thesis*, "Adaptive Explicitly Parallel Instruction Computing" May 2001, New York University.

3. A. Leung and S. Talla, *Harold Grad Prize*, April 1998 *and Dean's Dissertation Fellowship*, September 1999, respectively, New York University.

V. OTHER SCHOLARLY ACCOMPLISHMENTS

1. Chaired the co-development of the Trimaran system (www.trimaran.org) and led international dissemination. Trimaran has been used at over 40 universities in seven countries (1997-2007).

2. Participated in the technology transfer of algorithms used in the ASTI module of the parallelizing front end in IBM's C and Fortran compilers (1991–1994).

VI. RECENT PROFESSIONAL CONTRIBUTIONS

Conference Organization and Editorial Activities

1. Member Steering Committee, *Symposium on Transformational Information Science and Engineering*, Nanyang Technological University, Singapore, January 28-29, 2010.

2. Program Co-chair (with Lin Zhong), *PRANACOMP 2008, The First Workshop on Probabilistic and Resilient Architectures for Nanoscale Computing 2008*, Rice University, Houston, TX. April 2-3, 2008.

3. Steering Committee member of *ACM-IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, 1999-present.

4. Founding steering committee member of *ACM-IEEE Embedded Systems Week* (*ESWEEK*), 2005-present.

5. Founder and Program Chair, *Workshop on Compiler-Assisted System-On-Chip Assembly (CASA)*, ESWEEK, 2007.

6. Associate Editor, *ACM Transactions on Embedded Computing Systems.*

7. Editor, *International Journal of Embedded Computing.*

8. Guest co-editor (with Wen-mei Hwu) of the *IEEE Transactions on Computers Special issue* in memory of B. Ramakrishna (Bob) Rau.

9. Program committee member, *International Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS)* 2005.

10. Program committee member, *International Symposium on High-Performance Computer Architecture (HPCA)*, 2006.

11. General Chair, *ACM-IEEE CASES 2001*, Atlanta, GA, 2001.

12. Program founder and chair, scientific advisory board on *Use Inspired Research: Initiative in Embedded and Hybrid Systems,* Agency for Science, Technology and Research (A-STAR), Singapore, August 2001 – August 2005.

13. Conference chair, *ACM-IEEE CASES 2000,* San Jose, CA, 2000.

14. Associate editor of *The IEEE Transactions on Parallel and Distributed Systems*, 1999 – 2003.

15. Founding Program co-chair (with Guang Gao), *CASES98, Workshop on Compiler and Architecture Support for Embedded Systems*, Washington, DC, October 1998; CASES has now evolved into an ACM-IEEE sponsored event and is one of the three anchor conferences of ESWEEK.

16. Associate editor, *Constraints: An International Journal*, Kluwer, 1995–present.

Panelist Activity

1. Agency for Science, Technology and Research, Singapore, 2001. Chair, *Emerging Directions in Embedded & Hybrid Systems.*

2. NSF-DARPA Workshop Embedded Systems Panel, Washington, DC, 2000. Chair, *Future Directions in Hybrid and Embedded Systems.*

3. National Science Foundation, Washington, DC, 1995. *Careers Panel.*

4. National Science Foundation, Washington, DC, 1994.
   Small Business Initiatives (SBIR) Panel Modeling Responsive Computing Systems: Compilation Issues.

5. National Science Foundation, Washington, DC, 1993 *Young Investigator (NYI) Award Panel.*

VII. SELECT KEYNOTE AND INVITED PRESENTATIONS

1. On "The End of Moore`s Law and the Future of Computing Systems, Probably" at *The Institute of Electronics, Information and Communication Engineers (IEICE), Technical Committee on Reconfigurable Systems*, Kitakyushu City, Japan, Nov 2008.

2. On "Probabilistic Low Energy Computing" at
    a. *Coolchips VII*, Sponsored by IEEE and ACM SIGARCH, Yokohama, Japan, Apr 2004.
    b. *International Conference on High Performance Computing*, Sponsored by IEEE and ACM SIGARCH, Hyderabad, India, Dec 2003.
    c. *Conference on Compilers, Architectures and Synthesis of Embedded Systems,* Sponsored by ACM SIGMICRO and IEEE, San Jose, CA, Oct 2003.
3. On **"**Adaptive EPIC Processors and Compilation Techniques," *Application-Specific Multi-Processor SoC, Summer school sponsored by IEEE Circuits and Systems Society and EDAA*, July, 2001, Aix-les-Bains, France.
4. NSF-DARPA Workshop on "Compilers, Architectures and Synthesis of Embedded Systems," Washington DC, October 2000.
5. "Trimaran: An Infrastructure for Research in Instruction Level Parallel Processing," (with Ben Goldberg, Hansoo Kim and other Trimaran participants at
    a. The 1998 Symposium on Parallel Architectures and Compiler Techniques (PACT), Paris, France, October 1998.
    b. The 1998 ACM Symposium on Programming Language and Implementation (PLDI), Atlanta, GA, May 1999.
    c. The School on Computational Aspects and Applications of Hybrid Systems, Grenoble, France, October 1998.

6. "Master Class in Reconfigurable Systems," Adelaide, Australia, September 1998.

VIII. AWARDS, GRANTS AND CONTRACTS

Awards from Industry

1. *Curricular Development Award*, Center for Research in Embedded Systems and Technology, Georgia Institute of Technology, Hewlett Packard Corporation, $816,616. One of two awarded internationally (1999).

2. *Panasonic Research Award*, 1997– 98, $100,000.

3. *Hewlett-Packard Research Award*, 1996–99, over $900,000 cash, and $400,000 equipment.

Other Grants and Contracts

1. *PACE: A Platform Aware Compilation Environment*, DARPA Contract, With Keith D. Cooper (PI), John Mellor-Crummey (Co-PI), Vivek Sarkar (Co-PI), Linda Torczon (Co-PI), Rice University, 2009-2014, US$ 16Million.[§]

2. *Institute for Sustainable Nanoelectronics (ISNE)*, Nanyang Technological University, Singapore, Krishna V. Palem, Director, Singapore $4Million, Aug 2008 – 2010.

3. *Probabilistic computing and biological applications*, NSF Computing and Communication Foundations, with David Anderson (PI), Paul Hasler (Co-PI), Robert Butera (Co-PI), US $ 750,000, Georgia Institute of Technology, Sep 2007-Aug 2010.

4. Total of over US $ 4,500,000 since 1999 - 2006 from Federal agencies (of which about US $ 2,300,000 includes Co-PI's A. Chatterjee, V. Mooney and S. Yalamanchili in different contracts)

IX. GRADUATE STUDENT SUPERVISION

INDIVIDUAL STUDENT GUIDANCE

Current Ph.D. Students

1. Scott Novich, Rice University, Department of Electrical and Computer Engineering
2. Kirthi Krishna Muntimadugu. Rice University, Department of Electrical and Computer Engineering
3. Avinash Lingamneni, Rice University, Department of Electrical and Computer Engineering
4. Charles Hardnett, Georgia Institute of Technology, College of Computing, "Loop Transformations for Locality Enhancement".
5. Allen Leung, New York University, "Compiler Optimizations and their Interactions with Garbage Collection with Applications to Java," Ph.D, began advising: September 1995, Status: Defended thesis March 2001; Pending final submission of dissertation.

[§] Includes sub-contracts with Rice University as the prime.

Graduated Ph.D. Students

1. Lakshmi Chakrapani, Georgia Institute of Technology, College of Computing, "Probabilistic Architectures", Graduated 2008, Employed: Rice University.
2. Pinar Korkmaz, Georgia Institute of Technology, School of Electrical & Computer Engineering, "Program Optimizations for Management Power in the Memory Subsystem," (joint with V. Mooney). Graduated 2007, Employed: Intel Corporation.
3. Rodric Rabbah, Georgia Institute of Technology, College of Computing, "Compiler Optimizations for Profile Based Management of the Memory Hierarchy," Graduated: 2006, Employed: IBM T. J. Watson Research Center.
4. Jinwoo Kim, Georgia Institute of Technology, College of Computing, "Hardware Support of Compiler Optimizations for Smart Cache Management," Graduated: 2003. Employed: City University of New York, New York, N.Y
5. Suren Talla, New York University, Courant Institute, "Adaptive EPIC Architectures and their Compilers," Ph.D., Graduated May 2001. Employed: StarCore, Atlanta, GA.
6. Hansoo Kim, New York University, "Region Based Register Allocation," Ph.D., graduated August 2000. Employed: Citibank, New York, NY.
7. S. Muthukrishnan, New York University, "Algorithms for String and Pattern Matching," (joint with J. Spencer), Ph.D., Graduated: 1992, Employed: Rutgers University, New Brunswick, NJ.
8. P. Ouyang, New York University, "Compiling Regular Loops for Efficient Parallel Execution", Ph.D., Graduated: 1990, Employed: Synopsis Corporation, San Jose, CA.
9. L. Ke, New York University, "Rewriting Systems," Ph.D., Graduated: 1989, Employed: Fujitsu Corporation, San Jose, CA.

X. TEACHING

Curriculum Development, Rice University

1. Introduced a course in Spring 2009, *The Role of Chance in an Information World.* This course was intended to show that the concept of probability is a powerful idea pervading many aspects of our lives and has a surprisingly long history.

2. Introduced a seminar course in Spring 2009 (Co-instructor Dr. Christopher Bronk), *Sustainability, Energy, And Information Technology: An Interdisciplinary Approach.* This course targeted to answer the global society's great dilemmas—the increasingly high concentration of carbon and greenhouse gases in the Earth's

atmosphere and how Information Technology can play a role in addressing this problem.

Curriculum Development, Georgia Institute of Technology

As part of the Center for Research in Embedded Systems and Technology, a three-course sequence has been developed on Modern Computer Architecture, Optimizing Compilers, and in Pervasive Computing. The first two of these courses, i.e., architectures and compilers were taught first at New York University and are now offered at the Georgia Institute of Technology. *Compiler Design: Optimizations for Modern Processors* was offered during the Fall 2000 semester and *High Performance Computer Architecture: The EPIC Approach* was offered during the Spring semester 2001. The third course entitled, *Designing Pervasive Computing Environments,* was offered during the Fall 2001 semester. The courses are evaluated, sponsored, and co-developed with the Hewlett Packard Corporation.

1. **Designing Pervasive Computing Environments**, (ECE8833A, also cross-listed as a graduate course in the College of Computing as CS8803.)

2. **High Performance Computer Architecture: The EPIC Approach:** (ECE 8833, also cross-listed as a graduate course in the College of Computing as CS 8803K EPIC Architectures.)

3. **Compiler Design: Optimizations for Modern Processor:** (ECE 8833A, also cross-listed as a graduate course in the College of Computing as CS 6241 Compiler Design).

Curriculum Development, New York University

1. Introduced an advanced course, *Code Optimization in Modern Compilers*. This course was offered as G22.3033.01 *Optimizing Compilers* and G22.2131.001 *Advanced Topics In Compilers and* G22.3033.008 *Optimizing Compilers*. It is the basis for the Hewlett Packard Curriculum Development Award and is the foundation for the new course offered during the Fall 2000 semester at the Georgia Institute of Technology.

2. Developed a new Graduate Operating Systems course and 500 pages of lecture notes, jointly with Professor Malcolm Harrison.

3. Initially developed and offered as G22.3250.001 *Honors Operating Systems*, Fall 1996.

Short Courses

- Short course on "Code Optimization in Modern Compilers" offered at Tata Institute, Bombay, India, and with Vivek Sarkar, via the Western Institute of Computer Science, Stanford University, Palo Alto, 8/94, 8/95 and 8/96. This course was co-developed with V. Sarkar and served as the foundation for subsequent courses on optimizing compilers.

XI. SELECT CAMPUS CONTRIBUTIONS

Rice University Committee and Service Activities

1. *Computer Science Department Colloquium Committee*

2. *School of Engineering Tenure and Promotions Committee*

Georgia Institute of Technology Committee and Service Activities

3. *Seminar Committee*, 2000 – 2001.

4. *Farmer Chair* Search Committee, 2000 - 2003.

5. *Motorola Chair* Search Committee, 2001 – 2002.

6. Director, *Center for Research in Embedded Systems and Technologies* (CREST), 2000-present.

New York University Committee and Service Activities

1. *Graduate Student Fellowship* Committee, 1997 – 1998

2. *Faculty Appointments* Committee (Tenure and Promotions Committee), 1997 – 1999

XII. PUBLICATIONS

1. "Optimizing Energy to Minimize Errors in Dataflow Graphs Using Approximate Adders" with Zvi Kedem, Vincent Mooney, Kirthi Krishna Muntimadugu, Avani Devarasetty, Phani Deepak Parasuramuni, *International*

conference on Compilers, Architectures, and Synthesis for Embedded Systems, (CASES), Arizona, USA, 2010. *(To appear)*

2. "Compilers, Architectures and Synthesis for Embedded Computing: Retrospect and Prospect", *Record of IEEE Computer Society 2010 W. Wallace McDowell Award, International conference on Compilers, Architectures, and Synthesis for Embedded Systems*, (CASES), Arizona, USA, 2010. *(To Appear)*
3. "The Arrow of Time through the Lens of Computing", *Essays in Memory of Amir Pnueli, pp. 362-369*, 2010. *(Invited)*
4. "Probabilistic Arithmetic and Energy Efficient Embedded Signal Processing", with Jason George, Bo Marr and Bilge E. S. Akgul, *ACM Transactions on Embedded Computing systems. (To appear)*
5. "A Probabilistic Boolean Logic for Energy Efficient Circuit and System Design" with Lakshmi N. B. Chakrapani, *Proceedings of the 15th Asia and South Pacific Design Automation Conference* (ASPDAC), January, 2010.
6. "Sustaining moore's law in embedded computing through probabilistic and approximate design: retrospects and prospects" with Lakshmi N.B. Chakrapani, Zvi M. Kedem, Avinash Lingamneni, Kirthi Krishna Muntimadugu, *International conference on Compilers, Architectures, and Synthesis for Embedded Systems*, (CASES), Grenoble, France, 2009.
7. "I-Slate, Ethnomathematics and Rural Education" with Al Barr, Avinash Lingamneni, Vincent Mooney, Rajeswari Pingali, Harini Sampath, Jayanthi Sivaswamy, *IEEE Conference on Technologies for Humanitarian Challenges*, Bangalore, India, 2009.
8. "Probabilistic CMOS (PCMOS) Logic for Nanoscale Circuit Design" *International Solid State Circuits Conference: Advanced Solid-State Circuits Forum*, San Francisco, CA, February 2009.
9. "Highly Energy and Performance Efficient Embedded DSP through "Somewhat" Erroneous Arithmetic" with Lakshmi N. B. Chakrapani, Kirthi Krishna, Lingamneni Avinash, Jason George, *International conference on Compilers, Architectures, and Synthesis for Embedded Systems*, Atlanta, GA, 2008.
10. "Energy, Performance, and Probability Tradeoffs for Energy-Efficient Probabilistic CMOS Circuits" with Korkmaz, P, Akgul, B. E. S, *IEEE Transactions on Circuits and Systems, Volume 55(8), pp. 2249-2262*, September 2008.
11. "Hardware realization of a medical diagnostic system based on Probabilistic CMOS (PCMOS) technology" with Zhi-Hui Kong, Jun-Jie Tan, Akgul, B.E.S, Kiat-Seng Yeo, Wang-Ling Goh, *IEEE International Symposium on VLSI Design, Automation and Test*(VLSI-DAT), 2008.
12. "A fuzzy control chip based on Probabilistic CMOS technology" with Jian-Xin Xu, Chao Xue, Chang-Chieh Hang, *International Conference on Fuzzy Systems* (FUZZ-IEEE),2008. (IEEE World Congress on Computational Intelligence).
13. "Probabilistic Design: A Survey of Probabilistic CMOS Technology and Future Directions for Terascale IC Design" with Lakshmi N. B. Chakrapani, Jason George, Bo Marr, Bilge E. S. Akgul, *VLSI-SoC: Research Trends in*

VLSI and Systems on Chip, De Micheli, Giovanni; Mir, Salvador; Reis, Ricardo (Eds.), ISBN: 978-0-387-74908-2, December 2007.

14. "Analysis of probability and energy of nanometre CMOS circuits in presence of noise" with Korkmaz, P, Akgul, B.E.S *Electronics Letters, Volume 43(17), pp. 942-943,* August 2007.
15. "Probabilistic System-on-a-chip Architectures" with Lakshmi N. B. Chakrapani, Pinar Korkmaz, Bilge E. S. Akgul *ACM Transactions on Design Automation of Electronic Systems (ACM-TODAES) Volume 12(3),* August, 2007.
16. "Probabilistic CMOS Technology: A Survey and Future Directions", with Bilge E. S. Akgul, Lakshmi N. Chakrapani, Pinar Korkmaz *IFIP International Conference on Very Large Scale Integration (VLSI-SoC), 2006.*
17. "Probabilistic Arithmetic and Energy Efficient Embedded Signal Processing", with Jason George, Bo Marr and Bilge E. S. Akgul, *Proceedings of the Intl. Conference on Compilers, Architecture and Synthesis for Embedded Systems* (CASES), October 2006.
18. "Advocating Noise as an Agent for Ultra Low-Energy Computing: Probabilistic CMOS Devices and their Characteristics," with P. Korkmaz, B. E. S. Akgul and L. N. Chakrapani, *Japanese Journal of Applied Physics, SSDM Special Issue Part 1.*
19. "A Review on Probabilistic CMOS (PCMOS) Technology: From Device Characteristics to Ultra Low-Energy SoC Architectures," with L. N. Chakrapani, B. E. S. Akgul and P. Korkmaz, *High Performance Embedded Computing Handbook: A Systems Perspective.*
20. "Ultra Efficient Embedded SoC Architectures based on Probabilistic CMOS (PCMOS) Technology," with L. N. Chakrapani, B. E. S. Akgul, S. Cheemalavagu, P. Korkmaz and B. Seshasayee, *The Proceedings of The 9th Design Automation and Test in Europe (DATE),* March 2006.
21. "Ultra-low Energy Computing with Noise: Energy-Performance-Probability Trade-offs," with P. Korkmaz and B. E. S. Akgul, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Karlsruhe, Germany,* March 2006.
22. "A Probabilistic CMOS Switch and its Realization by Exploiting Noise," with S. Cheemalavagu, P. Korkmaz, B. E. S. Akgul and L. N. Chakrapani, *Proceedings of The IFIP-International Conference on Very Large Scale Integration, Perth, Australia,* October 2005.
23. "Data Trace Cache: An application specific cache architecture," with S. Ramaswamy, J. Sreeram and S. Yalamanchili, *2005 Workshop (Memory performance: Dealing with Applications, systems and architecture), Saint Louis, Missouri*, September 2005.
24. "The Explicit Use of Probability in CMOS Designs and the ITRS Roadmap: From Ultra-low Energy Computing to a Probabilistic Era of Moore's Law for CMOS (invited)," with B. E. S. Akgul, *Cavin's Corner at Semiconductor Research Corporation (SRC),* September 2005.
25. "Realizing Ultra-low Energy Application Specific SoC Architectures through Novel Probabilistic CMOS (PCMOS) Technology," with L. N. Chakrapani, B. E. S. Akgul and P. Korkmaz, *Proceedings of the 2005 International*

Conference on Solid State Devices and Materials (SSDM), Kobe, Japan, September 2005.

26. "Energy Aware Computing Through Probabilistic Switching: A Study of Limits," *IEEE Transactions on Computers Volume 54(9), pp. 1123-1137*, September 2005.
27. "A Framework For Compiler Driven Design Space Exploration For Embedded System Customization (invited)," with L. N. Chakrapani and S. Yalamanchili, *Proceedings of the Ninth Asian Computing Science Conference, In Lecture Notes in Computer Science, Springer-Verlag, Volume 3321, Pages 395-406*, December 2004.
28. "Ultra Low-energy Computing via Probabilistic Algorithms and Devices: CMOS Device Primitives and the Energy-Probability Relationship," with S. Cheemalavagu, P. Korkmaz, *Proceedings of The 2004 International Conference on Solid State Devices and Materials (SSDM)*, Tokyo, Japan, September 2004.
29. "Adaptive Compiler Directed Prefetching for EPIC Processors," with J. Kim, R.Rabbah, W. Wong, *International Multiconference in Computer Science and Computer Engineering*, Las Vegas, NV, June 2004.
30. "Low Energy Computing: From Novel Semiconductor Devices to Applications, Models, and Moore's Law (invited)," *Coolchips VII*, Yokohama, Japan, Apr 2004.
31. "Trimaran: An Infrastructure for Research in Instruction-Level Parallelism," with L. N. Chakrapani, J. C. Gyllenhaal, W-M. W. Hwu, S. A. Mahlke and R. M. Rabbah, *Proceedings for the 17th International Workshop on Languages and Compilers for Parallel Computing*, 2004, *In Lecture Notes in Computer Science, Springer-Verlag, Volume 3602, Pages 32-41*, 2005.
32. "Data Remapping for Design Space Optimization of Embedded Memory Systems," with R. Rabbah. *ACM Transactions on Embedded Systems, Volume: 2 (2) pages 186 – 218*, May 2003.
33. "Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices," *International Conference on High Performance Computing*, Hyderabad, India, Dec 2003. Also appeared as: "Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices," *Proceedings of The Intl. conference on compilers, architecture and synthesis for embedded systems (CASES)*, 2003.
34. "Energy minimization of a pipelined processor using a low voltage pipelined cache," with Park, J.C.; Mooney, V.J., III, K.; Kyu-won Choi. *Thirty-Sixth Asilomar Conference on Signals, Systems and Computers*, Nov 2002.
35. "Software Bubbles: Using Predication to Compensate for Aliasing in Software Pipelines," with B. Goldberg, E. Crutcher, C. Huneycutt, *International Conference on Parallel Architectures and Compilation Techniques (PACT*), September 2002.

36. "Proof as Experiment: Algorithms from a Thermodynamic Perspective", *Proceedings of The Intl. Symposium on Verification (Theory and Practice)*, Taormina, Sicily, Italy, July 2003.
37. "Design Space Optimization of Embedded Memory Systems via Data Remapping," with Rodric M. Rabbah, Vincent Mooney III, Pinar Korkmaz and Kiran Puttaswamy. *In Proceedings of the Languages, Compilers, and Tools for Embedded Systems and Software and Compilers for Embedded Systems (LCTES-SCOPES)*, June 2002.
38. "A Framework for Data Prefetching Using Off-Line Training of Markovian Predictors," with J. Kim, W. Wong. *20th International Conference on Computer Design*, Germany, 2002.
39. Power-Performance Trade-Offs in second level memory used by an ARM-Like RISC Architecture," with K. Puttaswamy, L. N. Chakrapani, K. W. Choi, Y. S. Dhillon, U. Diril, P. Korkmaz, K. K. Lee, J. C. Park, A. Chatterjee, P. Ellervee, V. Mooney and W. F. Wong in the book *Power Aware Computing*, edited by Rami Melhem, University of Pittsburgh, PA, USA and Robert Graybill, DARPA/ITO, Arlington, VA, USA, published by Kluwer Academic/Plenum Publishers, pp. 211-224, May 2002
40. The Emerging Power Crisis in Embedded Processors: What Can A Poor Compiler Do?," with L.N. Chakrapani, P. Korkmaz, V.J. Mooney III, and W.F. Wong, *Proc. of International Conference on Compilers, Architectures, and Synthesis of Embedded Systems,* Nov 2001.
41. "Compiler Optimizations for Adaptive EPIC Processors," with S. Talla, W. Wong. *First International Workshop on Embedded Software (EMSOFT)*, Tahoe City, CA, 2001.
42. "Connectivity Properties in Random Regular Graphs with Edge Faults", with S. Nikoletseas, P. Spirakis and M. Yung, *Special Issue on Randomized Computing of the International Journal of Foundations of Computer Science (IJFCS)*, 2000.
43. "Instruction Scheduling with Timing Constraints on Single RISC Processor with 0/1 Latencies," with H. Wu, J. Jaffar and R. Yap. *Sixth International Conference on Principles and Practice of Constraint Programming*, Singapore, 2000.
44. "Emerging Application Domains and the Computing Fabric (invited)," Advances in Computing Science - *ASIAN'99: 5th Asian Computing Science Conference, Phuket, Thailand*, December 1999.
45. "Adaptive Explicitly Parallel Instruction Computing," with S. Talla, P. Devaney, et.al., *Fourth Australasian Computer Architecture Conference*, Auckland, New Zealand, January 1999.
46. "Scheduling Time-Constrained Instructions in Pipelined Processors," with A. Leung and A. Pnueli. *ACM Transactions on Programming Languages and Systems, October* 2000. Also appeared as: "A Fast Algorithm for Scheduling Time-constrained Instructions in RISC Machines," *Proc. 1998 Symposium on Parallel Architectures and Compiler Techniques*, Paris, France, October 1998.
47. "TimeC: A Time Constraints Language for ILP Processor Compilation," with A. Leung and A. Pnueli, *Constraints*, August 2000. Also appeared as:

"TimeC: A Notation for Expressing Time-constraints in Programs,", *Proc. The Fifth Annual Australasian Conference on Parallel and Real-time Systems*, Adelaide, Australia, September 1998.

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