A Multi-core Parallelizing Compiler for Low-Power High-Performance Computing

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Hironori Kasahara

<Personal History>

<Activities for Societies>
IPSJ: Sig. Computer Architecture (Chair), Trans of IPSJ Editorial Board (HG Chair), Journal of IPSJ Editorial Board (HWG Chair), 2001 Journal of IPSJ Special Issue on Parallel Processing (Chair of Editorial Board: Guest Editor, JSPP2000 (Program Chair) etc.
ACM: International Conference on Supercomputing (ICS) (Program Committee) Int’l conf. on Supercomputing (PC, esp. ‘96 ENIAC 50th Anniversary Co-Prog. Chair).
IEEE: Computer Society Japan Chapter Chair, Tokyo Section Board Member, SC07 PC OTHER: PCs of many conferences on Supercomputing and Parallel Processing.

<Activities for Governments>
METI: IT Policy Proposal Forum (Architecture/HPC WG Chair), Super Advanced Electronic Basis Technology Investigation Committee NEDO: Millennium Project IT21 “Advanced Parallelizing Compiler” (Project Leader), Computer Strategy WG (Chair), Multicore for Realtime Consumer Electronics Project Leader etc.
MEXT: Earth Simulator project evaluation committee, 10PFLOPS Supercomputer evaluation comm.
JAERI: Research accomplishment evaluation committee, CCSE 1st class invited researcher.
JST: Scientific Research Fund Sub Committee, COINS Steering Committee, Precursory Research for Embryonic Science and Technology (Research Area Adviser)

<Papers> 151 Papers with Review, 20 Papers for Symposium with Review, 105 Technical Reports, 154 Papers for Annual Convention, 49 Invited Talks, 74 Articles in Newspaper & Web, etc.
Multi-core Everywhere

Multi-core from embedded to supercomputers

- **Consumer Electronics (Embedded)**
  Mobile Phone, Game, Digital TV, Car Navi, DVD, Camera
  IBM/ Sony/ Toshiba Cell, Fujitsu FR1000, NEC/ARM MPCore&MP211, Panasonic Uniphier, Renesas SH multi-core (RP1)

- **PCs, Servers**
  Intel Dual-Core Xeon, Core 2 Duo, Montecito
  AMD Quad and Dual-Core Opteron

- **WSs, Deskside & Highend Servers**
  IBM Power4, 5, 5+, pSeries690(32way), p5 550Q(8 way), Sun Niagara(SparcT1, T2), SGI ALTIX350,

- **Supercomputers**
  IBM Blue Gene/L: **360TFLOPS**, 2005,
  Low power CMP based 128K processor chips

High quality application software, Productivity, Cost performance, Low power consumption are important
Ex, Mobile phones, Games

Compiler cooperated multi-core processors are promising to realize the above futures
Market of Consumer Electronics
1 Trillion Dollars in 2010 (World Wide)

Annual Growth Rates

<table>
<thead>
<tr>
<th>Product</th>
<th>'03</th>
<th>'07</th>
<th>Annual Average Growth Rate %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dig. Camera</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>デジタルスチルカメラ（M台）</td>
<td>49</td>
<td>76</td>
<td>12</td>
</tr>
<tr>
<td>Dig. TV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>デジタルTV（M台）</td>
<td>6</td>
<td>27</td>
<td>45</td>
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<tr>
<td>DVD Recorder</td>
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<td></td>
<td></td>
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<tr>
<td>DVDレコーダ（M台）</td>
<td>3.6</td>
<td>33</td>
<td>74</td>
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<tr>
<td>DVD for PC</td>
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<tr>
<td>PC用DVD（記録型）（M台）</td>
<td>27</td>
<td>114</td>
<td>43</td>
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<tr>
<td>Mobile Phone</td>
<td></td>
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<td></td>
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<tr>
<td>携帯電話（M台）</td>
<td>490</td>
<td>670</td>
<td>8</td>
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<tr>
<td>LSI for Cars</td>
<td></td>
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<td></td>
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<tr>
<td>自動車用半導体需要（BS）</td>
<td>14.0</td>
<td>20.9</td>
<td>11</td>
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</table>
Roadmap of compiler cooperative multicore project

00 01 02 03 04 05 06 07 08 09 10

Millennium Project IT21
NEDO Advanced Parallelizing Compiler
(Waseda Univ. Fujitsu, Hitachi, JIPDEC, AIST)

STARC Compiler Cooperative Chip Multiprocessor
(Waseda Univ., Fujitsu, NEC, Toshiba, Panasonic, Sony)

NEDO (2004.07-2007.06)
Heterogeneous Multiprocessor
(Waseda Univ., Hitachi)

NEDO (2005.06-2008.03)
Multicore Technology for Realtime Consumer Electronics
Waseda Univ., Hitachi, Renesas, Fujitsu, NEC, Toshiba, Panasonic
Power Saving Multicore Architecture, Parallelizing Compiler, API

NEDO (2007.02-2010.03)
Heterogeneous Multicore for Consumer Electronics Waseda Univ., Hitachi, Renesas, Tokyo Inst. of Tech.

Apply for Supercomputer Compilers

Compiler development of Multiprocessor Servers

Basic research

Practical research

Plan
Arch. & Compiler R&D
Practical Use

Soft realtime

Plan
Multicore Arch. Compiler API R&D
Practical Use

Plan
Hetero Multicore Arch. & Compiler R&D

STARC: Semiconductor Technology Academic Research Center
Fujitsu, Toshiba, NEC, Renesas, Panasonic, Sony etc.

Waseda Univ., Hitachi, Renesas,
METI/NEDO National Project
Multi-core for Real-time Consumer Electronics

<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

<Period> From July 2005 to March 2008

<Features> • Good cost performance
• Short hardware and software development periods
• Low power consumption
• Scalable performance improvement with the advancement of semiconductor
• Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API: Application Programming Interface

(2005.7〜2008.3)**

**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC
METI/NEDO Advanced Parallelizing Compiler Technology Project

Millenium Project IT21 2000.9.8 –2003.3.31
Waseda Univ., Fujitsu, Hitachi, AIST

Background and Problems
① Adoption of parallel processing as a core technology on PC to HPC
② Increase of importance of software on IT
③ Need for improvement of cost-performance and usability

Contents of Research and Development
① R & D of advanced parallelizing compiler
   Multigrain, Data localization, Overhead hiding
② R & D of Performance evaluation technology for parallelizing compilers

Goal: Double the effective performance

Ripple Effect
① Development of competitive next generation PC and HPC
② Putting the innovative automatic parallelizing compiler technology to practical use
③ Development and market acquisition of future single-chip multiprocessors
④ Boosting R&D in the following many fields:
   IT, Bio-tech., Device, Earth environment,
   Next-generation VLSI design, Financial engineering,
   Weather forecast, New clean energy, Space development, Automobile, Electric Commerce, etc
Performance of APC Compiler on IBM pSeries690 16 Processors High-end Server

- IBM XL Fortran for AIX Version 8.1
  - Sequential execution: -O5 -qarch=pwr4
  - Automatic loop parallelization: -O5 -qsmp=auto -qarch=pwr4
  - OSCAR compiler: -O5 -qsmp=noauto -qarch=pwr4 (su2cor: -O4 -qstrict)

3.5 times speedup in average
OSCAR Parallelizing Compiler

- Improve effective performance, cost-performance and productivity and reduce consumed power
  - Multigrain Parallelization
    - Exploitation of parallelism from the whole program by use of coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism
  - Data Localization
    - Automatic data distribution for distributed shared memory, cache and local memory on multiprocessor systems.
  - Data Transfer Overlapping
    - Data transfer overhead hiding by overlapping task execution and data transfer using DMA or data pre-fetching
  - Power Reduction
    - Reduction of consumed power by compiler control of frequency, voltage and power shut down with hardware supports.
Generation of Coarse Grain Tasks

- **Macro-tasks (MTs)**
  - Block of Pseudo Assignments (BPA): Basic Block (BB)
  - Repetition Block (RB): outermost natural loop
  - Subroutine Block (SB): subroutine
Earliest Executable Condition Analysis for coarse grain tasks (Macro-tasks)
Automatic processor assignment in 103.su2cor

- Using 14 processors
  - Coarse grain parallelization within DO400 of subroutine LOOPS
MTG of Su2cor-LOOPS-DO400

- Coarse grain parallelism PARA_ALD = 4.3
Data-Localization

Loop Aligned Decomposition

- Decompose multiple loop (Doall and Seq) into CARs and LRs considering inter-loop data dependence.
  - Most data in LR can be passed through LM.
  - LR: Localizable Region, CAR: Commonly Accessed Region
Inter-loop data dependence analysis in TLG

- Define exit-RB in TLG as Standard-Loop
- Find iterations on which a iteration of Standard-Loop is data dependent
  - e.g. $K_{th}$ of RB3 is data-dependent on $K-1_{th}, K_{th}$ of RB2, on $K-1_{th}, K_{th}, K+1_{th}$ of RB1

Example of TLG
Decomposition of RBs in TLG

- Decompose GCIR into DGCIR\(p\)\((1 \leq p \leq n)\)
  - \(n\): (multiple) num of PCs,  DGCIR: Decomposed GCIR
- Generate CAR on which DGCIR\(p\)&DGCIR\(p+1\) are data-dep.
- Generate LR on which DGCIR\(p\) is data-dep.
Data Localization Group

MTG

MTG after Division

A schedule for two processors
An Example of Data Localization for Spec95 Swim

(a) An example of target loop group for data localization

(b) Image of alignment of arrays on cache accessed by target loops

Cache line conflicts occurs among arrays which share the same location on cache
Data Layout for Removing Line Conflict Misses by Array Dimension Padding

Declaration part of arrays in spec95 swim

**before padding**

```
PARAMETER (N1=513, N2=513)

COMMON U(N1,N2), V(N1,N2), P(N1,N2),
  * UNEW(N1,N2), VNEW(N1,N2),
  1 PNEW(N1,N2), UOLD(N1,N2),
  * VOLD(N1,N2), POLD(N1,N2),
  2 CU(N1,N2), CV(N1,N2),
  * Z(N1,N2), H(N1,N2)
```
APC Compiler Organization

APC Multigrain Parallelizing Compiler

- Source Program
  FORTRAN

Data Dependence Analysis
- Inter-procedural
- Conditional

Automatic Data Distribution
- Cache optimization
- DSM optimization

Multigrain Parallelization
- Hierarchical Parallel
- Affine Partitioning

Scheduling
- Static Scheduling
- Dynamic Scheduling

Speculative Execution
- Coarse Grain
- Medium Grain
- Architecture Support

OpenMP Code Generation

Feedback-directed Selection Technique of Compiler Directives
- Techniques for Profiling & Utilizing Runtime Info

Parallelizing Tuning System

Program Visualization Technique

Feedback

Variety of Shared Memory Parallel machines

SUN Ultra 80
IBM RS6000
20p Series 690
IBM XL Fortran Ver.8.1
IBM XL Fortran Ver.7.1
Sun Forte 6 Update 2
Image of Generated OpenMP Code for Hierarchical Multigrain Parallel Processing

1st layer

Distributed scheduling code

2nd layer

Thread group0

Thread group1

Centralized scheduling code
Performance of Multigrain Parallel Processing for 102.swim on IBM pSeries690

![Graph showing speed up ratio with processors on the x-axis and speed up ratio on the y-axis. Two lines represent XLF(AUTO) and OSCAR.]
Performance OSCAR Multigrain Parallelizing Compiler on a IBM p550q 8core Deskside Server

- 2.7 times speedup against loop parallelizing compiler on 8 cores

- Loop parallelization
- Multigrain parallelization

![Chart showing speedup ratio for various benchmarks]
OSCAR Compiler Performance on 24 Processor IBM p690Highend SMP Server

4.82 times speedup against loop parallelization
Performance on SGI Altix 450
Montecito 16 processors cc-NUMA server

- OSCAR compiler gave us 1.86 times speedup against Intel Fortran Itanium Compiler revision 8.1
NEC/ARM MPCore Embedded 4 core SMP

3.48 times speedup by OSCAR compiler against sequential processing
Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode

- Realtime processing mode with dead line constraints
OSCAR Multi-Core Architecture

CMP<sub>0</sub> (chip multiprocessor 0)

- CPU
- PE<sub>0</sub>
- PE<sub>1</sub>
- PE<sub>n</sub>
- LPM/ I-Cache
- LDM/ D-cache
- DSM
- DTC
- Network Interface
- Intra-chip connection network (Multiple Buses, Crossbar, etc)
- CSM / L2 Cache
- FVR

Inter-chip connection network (Crossbar, Buses, Multistage network, etc)

- CSM: central shared mem.
- DSM: distributed shared mem.
- DTC: Data Transfer Controller
- LDM : local data mem.
- LPM : local program mem.
- FVR: frequency / voltage control register
An Example of Machine Parameters for the Power Saving Scheme

• Functions of the multiprocessor
  – Frequency of each proc. is changed to several levels
  – Voltage is changed together with frequency
  – Each proc. can be powered on/off

<table>
<thead>
<tr>
<th>state</th>
<th>FULL</th>
<th>MID</th>
<th>LOW</th>
<th>OFF</th>
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<tr>
<td>frequency</td>
<td>1</td>
<td>1/2</td>
<td>1/4</td>
<td>0</td>
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<tr>
<td>voltage</td>
<td>1</td>
<td>0.87</td>
<td>0.71</td>
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<tr>
<td>dynamic energy</td>
<td>1</td>
<td>3/4</td>
<td>1/2</td>
<td>0</td>
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<tr>
<td>static power</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
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</table>

• State transition overhead

<table>
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<th>state</th>
<th>FULL</th>
<th>MID</th>
<th>LOW</th>
<th>OFF</th>
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<tbody>
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<td>40k</td>
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<tr>
<td>MID</td>
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<td>LOW</td>
<td>40k</td>
<td>40k</td>
<td>0</td>
<td>80k</td>
</tr>
<tr>
<td>OFF</td>
<td>80k</td>
<td>80k</td>
<td>80k</td>
<td>0</td>
</tr>
</tbody>
</table>

delay time [u.t.]  energy overhead [μJ]
Speed-up in Fastest Execution Mode

![Speed-up Bar Chart](chart.png)

- **Benchmark**: tomcatv, swim, applu, mpeg2enc
- **Speed-up Ratio**
  - w/o Saving
  - w Saving
Consumed Energy in Fastest Execution Mode

The chart shows the energy consumption in joules (J) and millijoules (mJ) for different benchmarks and numbers of processors. The x-axis represents the number of processors (1, 2, 4), and the y-axis represents the energy consumption. The chart compares 'w/o Saving' and 'w Saving' conditions.
Energy Reduction by OSCAR Compiler in Real-time Processing mode (1% Leak)

- deadline = sequential execution time, Leakage Power: 1%

- 82.7%
- 85.6%
- 86.7%
- 74.0%
Energy Reduction by OSCAR Compiler in Real-time Processing mode (10% Leak)

- deadline = sequential execution time, Leakage Power: 10%
Energy Reduction VS. Leakage Power (4 cores)

- deadline = sequential execution time*0.5
NEDOMulticore Technology for Realtime Consumer Electronics
R&D Organization(2005.7-2008.3)

Integrated R&D Steering Committee
Chair: Hironori Kasahara (Waseda Univ.), Project Leader
Sub-chair: Kunio Uchiyama (Hitachi), Project Sub-leader

Grant: Multicore Architecture and Compiler
Research and Development
Project Leader:
Prof. Hironori Kasahara, Waseda Univ.

R&D Steering Committee

Architecture & Compiler
R&D Group.
Group Leader:
Associate Prof. Keiji Kimura, Waseda Univ.
(Outsourcing: Fujitsu)

Standard Multicore
Architecture & API
Committee
Chair: Prof. Hironori Kasahara, Waseda Univ.

Subsidy: Evaluation Environment for Multicore Technology
Project Sub-leader:
Dr. Kunio Uchiyama, Chief Researcher, Hitachi

Test Chip
Development Group.
Group Leader:
Renesas Technology

Evaluation Sytem
Development Group
Group Leader:
Hitachi

Hitachi, Fujitsu, Toshiba, NEC,
Panasonic, Renesas Technology
Fujitsu FR-1000 Multicore Processor

FR-V Multi-core Processor

- FR550 core
- Mem. Cont.
- Memory

DMA-E
Local BUS IF

Fast I/O Bus
- Memory Bus: 64bit x 2ch / 266MHz
- System Bus: 64bit / 178MHz

FR550 VLIW Processor

- I-cache 32KB
- D-cache 32KB

Integer Operation Unit
- GR
- Inst. 0
- Inst. 1
- Inst. 2
- Inst. 3
- Inst. 4
- Inst. 5
- Inst. 6
- Inst. 7

Media Operation Unit

IO Chip

Crossbar Switch

Memory

Bus

Core1
Core2
Switch

Crossbar (FR1000)
Panasonic UniPhier

Scalable media processing architecture

1. UniPhier Processor for Mobile Phones
2. UniPhier Processor for Portable AV
3. UniPhier Processor for Car AV and Home Entertainment

Boosted speed and parallelism

CPU
UniPhier processor
Stream I/O
Memory control
AV I/O

With DPP extension

Execution units
Instruction cache
Data cache
Accelerator
Hardware engine

Instruction RAM
Data RAM

Execution unit array
Computing unit array
DPP

Hardware engine
CELL Processor Overview

- **Power Processor Element (PPE)**
  - PowerCore processes OS and Control tasks
  - 2-way Multi-threaded
- **Synergistic Processor Element (SPE)**
  - 8 SPE offers high performance
  - Dual issue RISC Architecture
  - 128bit SIMD(16 - way)
  - 128 x 128bit General Registers
  - 256KB Local Store
  - DedicatedDMA engines
1987 OSCAR (Optimally Scheduled Advanced Multiprocessor)
OSCAR (Optimally Scheduled Advanced Multiprocessor)
OSCAR PE (Processor Element)

SYSTEM BUS

BUS INTERFACE

LOCAL BUS 1  LOCAL BUS 2

DMA  LPM  DSM  DSM  LPM  DMA

INSTRUCTION BUS

INS C

DP

DMA : DMA CONTROLLER
LPM : LOCAL PROGRAM MEMORY (128KW * 2BANK)
INS C : INSTRUCTION CONTROL UNIT
DSM : DISTRIBUTED SHARED MEMORY (2KW)
LSM : LOCAL STACK MEMORY (4KW)

LD M : LOCAL DATA MEMORY (256KW)
DP : DATA PATH
IPU : INTEGER PROCESSING UNIT
FP U : FLOATING PROCESSING UNIT
REG : REGISTER FILE (64 REGISTERS)
OSCAR Multi-Core Architecture

CMP₀ (chip multiprocessor 0)

CPU

PE₀

PE₁

PEₙ

LPM/ I-Cache

LDM/ D-cache

DTC

DSM

Network Interface

Intra-chip connection network (Multiple Buses, Crossbar, etc)

CSM / L2 Cache

Inter-chip connection network (Crossbar, Buses, Multistage network, etc)

CSM: central shared mem.

LDM: local data mem.

DSM: distributed shared mem.

LPM: local program mem.

DTC: Data Transfer Controller

FVR: frequency / voltage control register

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API and Parallelizing Compiler in METI/NEDO
Advanced Multicore for Realtime Consumer Electronics Project

Sequential Application Program
(Subset of C Language)

Realtime Consumer Electronics Application Programs
Image, Secure Audio Streaming etc.

API to specify data assignment, data transfer, power reduction control

Translate into parallel codes for each vendor

Executable codes for each vendor chip

Backend compiler
API decoder Sequential Compiler

Mach. Codes

SH multicore
FR-V
(CELL)

Waseda OSCAR Compiler

Proc0 Scheduled Tasks
T1 Stop

Proc1 Scheduled Tasks
T2 T4

Proc2 Scheduled Tasks
T3 T6 Slow

Data Transfer by DTC(DMAC)
OSCAR Multigrain Parallelizing Compiler

- **Automatic Parallelization**
  - Multigrain Parallel Processing
  - Data Localization
  - Data Transfer Overlapping
  - Compiler Controlled Power Saving Scheme

- **Compiler cooperative Multi-core architecture**
  - OSCAR Multi-core Architecture
  - OSCAR Heterogeneous Multiprocessor Architecture

- **Commercial SMP machines**
Performance of OSCAR Compiler Using Memory Management API on SGI Altix450 Montecito CC-NUMA Server

Using SPEC95 tomcatv
Processor Block Diagram

CCN: Cache controller
IL, DL: Instruction/Data local memory
URAM: User RAM
GCPG: Global clock pulse generator
LCPG: Local CPG for each core
LBSC: SRAM controller
DBSC: DDR2 controller

On-chip system bus (SHwy)

300MHz

600MHz

Core #3
Core #2
Core #1
Core #0

CPU FPU
I$ 32K CCN D$ 32K
IL 8K DL 16K
URAM 128K

LCPG 0-3

URAM 128K

GCPG

LBSC DBSC HW IP PCI Exp

SRAM 32bit DDR2 32bit 4 lane
### Chip Overview

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
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<tbody>
<tr>
<td>Process Technology</td>
<td>90nm, 8-layer, triple-Vth, CMOS</td>
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<tr>
<td>Chip Size</td>
<td>97.6mm² (9.88mm x 9.88mm)</td>
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<tr>
<td>Supply Voltage</td>
<td>1.0V (internal), 1.8/3.3V (I/O)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.6 mW/MHz/CPU @ 600MHz (90nm G)</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>600MHz</td>
</tr>
<tr>
<td>CPU Performance</td>
<td>4320 MIPS (Dhrystone 2.1)</td>
</tr>
<tr>
<td>FPU Performance</td>
<td>16.8 GFLOPS</td>
</tr>
<tr>
<td>I/D Cache</td>
<td>32KB 4way set-associative (each)</td>
</tr>
<tr>
<td>ILRAM/OLRAM</td>
<td>8KB/16KB (each CPU)</td>
</tr>
<tr>
<td>URAM</td>
<td>128KB (each CPU)</td>
</tr>
<tr>
<td>Package</td>
<td>FCBGA 554pin, 29mm x 29mm</td>
</tr>
</tbody>
</table>

ISSCC07 Paper No.5.3, Y. Yoshida, et al., “A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption”
Performance on a Developed SH Multi-core (RP1: SH-X3) Using Compiler and API

Audio AAC* Encoder

Image Susan Smoothing

*) ISO Advanced Audio Coding
**) Mibench Embedded application benchmark by Michigan Univ.
OSCAR Heterogeneous Multicore

- OSCAR Type Memory Architecture
- LPM
  - Local Program Memory
- LDM
  - Local Data Memory
- DSM
  - Distributed Shared Memory
- CSM
  - Centralized Shared Memory
    - On Chip and/or Off Chip
- DTU
  - Data Transfer Unit
- Interconnection Network
  - Multiple Buses
  - Split Transaction Buses
  - CrossBar …
Static Scheduling of Coarse Grain Tasks for a Heterogeneous Multi-core
An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control

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<th>CPU1</th>
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<th>CPU3</th>
<th>DRP0</th>
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MTG1

MTG2

MTG3

TIM
Compiler Performance on a OSCAR Hetero-multi-core

- 25.2 times speedup using 4 SH general purpose cores and 4 DRP accelerators against a single SH core (Comparable Performance with 3GHz high performance processor by 300MHz low power multicore)

41.3 times Speedup

25.2 times Speedup against 1SH core
Power Reduction by OSCAR Compiler (4SHs + 4DRPs)

0.78 W: 22% Power reduction by Compiler Control
Conclusions

- Compiler cooperative low power high effective performance multi-core processors will be more important in wide range of information systems from games, mobile phones, automobiles to peta-scale supercomputers.

- Parallelizing compilers are essential for realization of
  - Good cost performance
  - Short hardware and software development periods
  - Low power consumption
  - High software productivity
  - Scalable performance improvement with advancement in semiconductor integration technology

- Key technologies in multi-core compiler
  - Multigrain parallelization, Data localization, Data transfer overlapping using DMA, Low power control technologies